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Article

Inverting tristate step-up converter

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Abstract: The here-treated step-up converter with two interference possibilities has several interesting features. First, the output voltage is inverse to the input voltage; second, the voltage transformation ratio is linearized; third, the dynamic behavior is that of a phase-minimum system; and fourth, the stress of the electronic switches is reduced. The function of the converter is explained, the steady state is presented, the large and small signal models are derived, and the Bode plots concerning the output voltage around the operating point are given. The start-up is investigated. Dimensioning hints are given. LTSpice is used to check the considerations.

Keywords: DC/DC converter; inverting step-up; modelling; transfer function; tristate

1. Introduction

DC/DC converters are important building blocks in modern technical systems. They are treated in detail in all the basic textbooks on Power Electronics. As examples, three valuable books are referenced here: Zach's book with more than 3400 pages [1], Mohan et al. [2] and Rozanov [3]. The basic idea of these converters is that energy is stored into an inductor during the on-time of an electronic switch, and during the off-time of this electronic switch, energy is taken from this coil and transferred to the output of the converter. One can distinguish between step-up, step-down, and step-up-down converters. When the output voltage is inverse to the input voltage, the converter is called an inverting one. Depending on the number of storage elements n (these are the inductors and the capacitors that have to store energy and are not used as resonant elements), the converter is called an n-order converter. Besides the basic converters treated in the textbooks, there are numerous other topologies. A famous basic study is the paper of Cuk [4]. Forouzeh et al. [5] produced an exhaustive review concerning step-up converters. Maksimovic and Cuk [6] wrote a starting text concerning converters that have a quadratic term of the duty cycle in the voltage transformation ratio.

Williams [7] summarizes more than 100 DC/DC converters. Marquez and Contreras-Ordaz [8] treat converters with three terminals. These converter topologies enable us to use more than one input voltage and/or load. Interleaved converters are especially interesting for higher power levels because power stages are here combined. As an example, the scientific report by Hosseinpour et al. shall be mentioned [9]. Banai and Bonab [10] proposed and treated a noninverting Buck-Boost converter with a higher voltage transformation ratio. Converters with extremely high switching frequencies lead to very compact designs. As an example, the study done by Mishima et al. [11] is mentioned. All these books and papers have additional references.

The starting point of this investigation is the paper of Colalongo et al. [12] which treats a step-up converter with reduced voltage stress across the electronic switch and

has a modified voltage transformation ratio. Liu and Ye [13] have shown this concept. Liu [14] presented similar converter concepts. These concepts are interesting but have the disadvantage that the intermediate capacitor is charged, when the main active switch turns on, by a peak current which can be very high when the converter is connected to a stable input source or has an input capacitor to avoid an overvoltage across the semiconductors caused by the parasitic input inductance. Himmelstoss [15] has shown, that the converter can be improved by a small additional inductor. Himmelstoss et al. applied this improvement to the inverting Luo step-up converter in [16]. In this paper the tristate concept is applied to this topology. **Figure 1** shows the original inverting super-lift converter published by Luo [17].

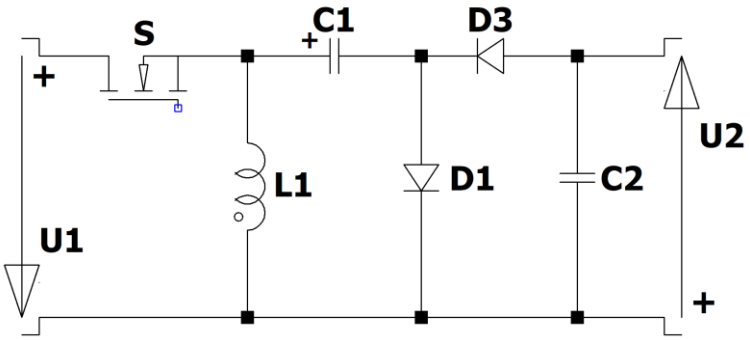


Figure 1. Original inverting boost converter according to Luo and Ye [17].

It can be easily seen that, when the input voltage is stable, the intermediate capacitor C1 is charged to the input voltage when the electronic switch S turns on. When the transistor is off, the current through the inductor L1 is discharging C1 and the voltage across it is decreasing. When the transistor is turned on again, a peak current recharges the capacitor. This is not advantageous, especially for the capacitor, but also for the input capacitor between the input terminals which avoids the overvoltage across the switch when turning off. It also stresses the electronic switch S and the diode D1. A small inductor L2 marked by the rectangle in **Figure 2** in series with the diode D1 damps the recharging process and produces a sinusoidal waveform. The circuit diagram is shown in **Figure 2**.

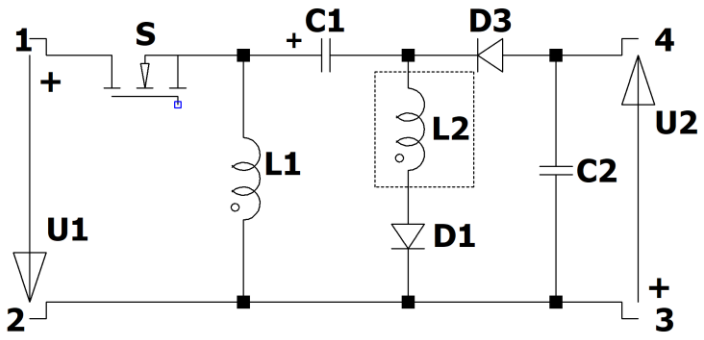


Figure 2. Improved inverting boost converter.

The tristate extension was originally proposed for the Boost converter by Viswanathan et al. [18–20]. The main electronic switch S of the converter is replaced by a series connection of two active switches S1 and S2. An additional diode D2 is

connected to the connection point of the two electronic switches. The other terminal of the diode is connected to the second connection point of the main inductor L1. The circuit diagram is shown in **Figure 3**. S2 and D2 are marked by a rectangle in **Figure 3**.

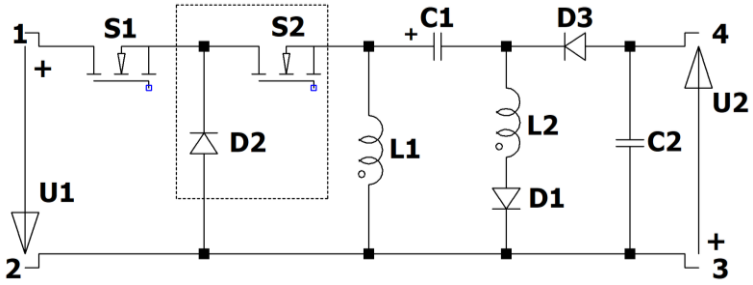


Figure 3. Tristate improved inverting boost converter.

As will be shown in the paper, this change in the topology leads to a linearization of the voltage transformation ratio when the duty cycle of S2 is held constant and is higher than the duty cycle of switch S1, and additionally when the duty cycle of switch S1 is used as a variable. Furthermore, the system is changed into a phase-minimum system.

2. Basic description

The function of the converter is described for ideal components; that means no resistors and ideal switching behavior in the steady state, continuous inductor current of L1, and when the output capacitor C2 is so large that the voltage across it nearly does not change during one period. There are three modes of operation. In mode M1, both active switches are on and the diodes D2 and D3 are off. In mode M2, S1 is off and the current through the main inductor L1 commutates into D2. During mode M3, both active switches are off and the diode D2 is now on.

2.1. Mode M1

Both switches are turned on and across the diode D3, there is a negative voltage of about the value of the output voltage. The load is supplied by the output capacitor C2. Across the main inductor L1, there is now the input voltage, and the current through it increases. A resonant current flows through C1 and L2 and charges the capacitor up to about the input voltage (in the ideal case, a little bit higher). When the resonant current reaches zero, the diode D1 turns off. One should dimension the resonant current so that the current reaches zero within the shortest on-time of switch S1.

During this mode the recharging of C1 occurs. The capacitor is discharged to $(U_1 - \Delta u_{C1})$ at the end of M3. Neglecting the parasitic resistors in the loop one gets with Kirchhoff's voltage law (KVL):

$$U_1 = \frac{1}{C_1}\int_0^t i_{L2}dt + (U_1 - \Delta u_{C1}) + L\frac{di_{L2}}{dt} + V_D \quad (1)$$

One gets for the current through the inductor L2:

$$i_{L2} = (\Delta u_{C1} - V_D)\sqrt{\frac{C_1}{L_2}}\sin\frac{1}{\sqrt{C_1 L_2}}t \tag{2}$$

The period of this ringing is given by:

$$T_U = 2\pi\sqrt{C_1 L_2} \tag{3}$$

The current reaches zero again after:

$$T_Z = \pi\sqrt{C_1 L_2} \tag{4}$$

This time must be smaller than the minimum on-time of the switch S1:

$$T_{on,\min} = d_{1,\min} T > \pi\sqrt{C_1 L_2} \tag{5}$$

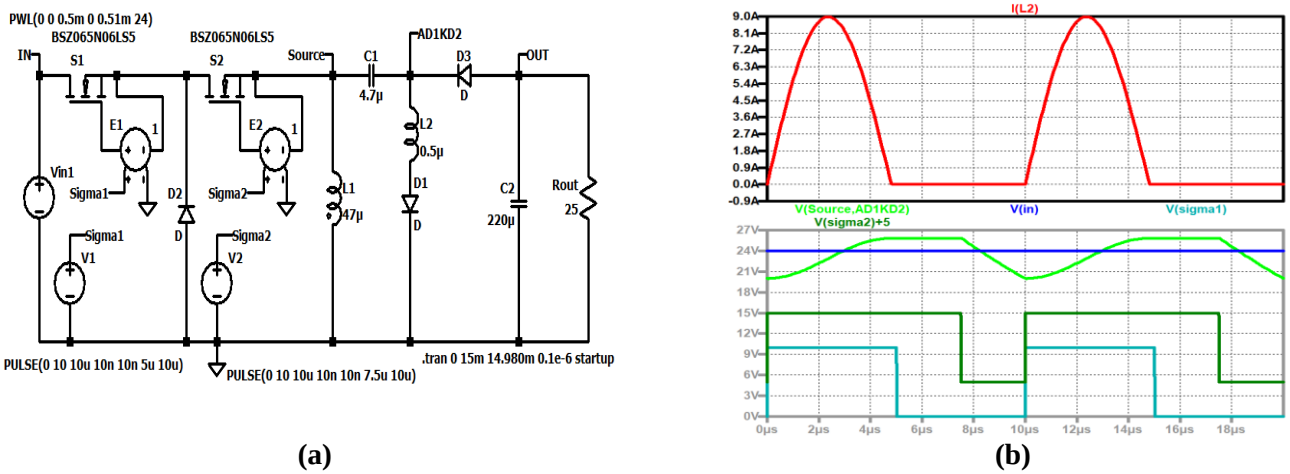
The peak current can immediately be found from Equation (2) according to:

$$\hat{I}_{L2} = (\Delta u_{C1} - V_D)\sqrt{\frac{C_1}{L_2}} \tag{6}$$

This resonant current charges the capacitor C1 up to:

$$u_{C1}(\pi\sqrt{C_1 L_2}) = \frac{1}{C_1}\int_0^{\pi\sqrt{C_1 L_2}} i_{L2}\,dt + (U_1 - \Delta u_{C1}) = \Delta u_{C1} - 2V_D + U_1 \tag{7}$$

Figure 4 shows the recharging process. The current has the form of a sinusoidal half-wave, and the voltage across C1 is oscillating around the input voltage. The voltage across the intermediate capacitor changes between 19.8 V and 26 V.



(a) **(b)**

Figure 4. Recharging process, **(a)** simulation circuit; **(b)** up to down: Current through the auxiliary coil L2 (red); voltage across C1 (green), input voltage (blue), control signal of switch S2 (dark green, shifted), control signal of switch S1 (turquoise).

2.2. Mode M2

Mode M2 starts when the electronic switch S1 is turned off. The current through the inductor L1 turns on the diode D2, and the voltage across the coil is now nearly zero and the current is nearly constant (in the ideal case it is constant). The voltage

across the diode D3 is still negative and has the value: Negative output voltage plus the voltage across C1, which is equal to about the input voltage. The load is still supplied by the output capacitor C2.

2.3. Mode M3

Mode M3 starts when the second switch is turned off, too. The current through the main coil commutates into the diode D3. The intermediate capacitor now discharges and the output capacitor gets charged. The voltage across the main inductor is now negative and the current through it decreases. The voltage is about the difference between the input voltage and the output voltage.

2.4. Voltage transformation ratio

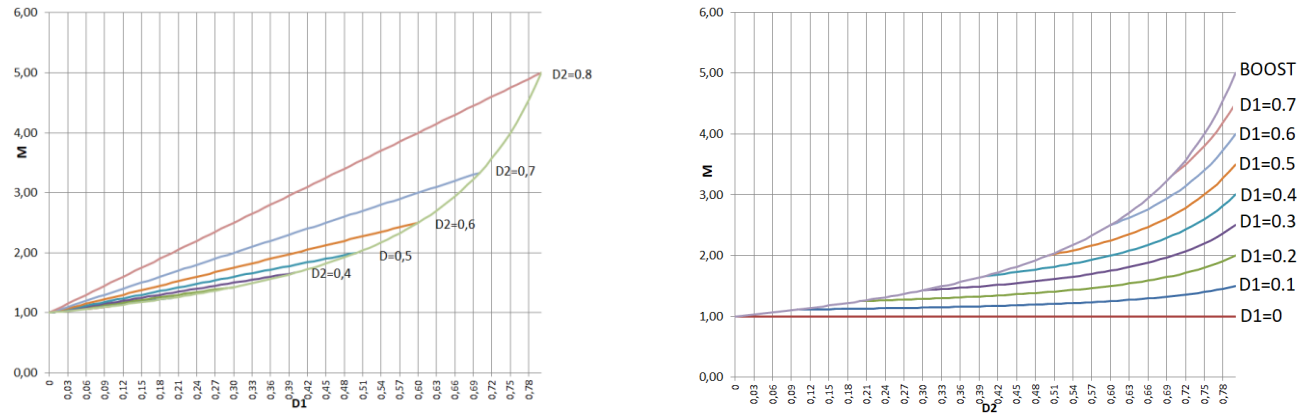
To obtain the voltage transformation ratio, one has to use the fact that in the steady state, the voltage across an inductor must be zero in the mean. The voltage across C1 is equal to the input voltage U1. Using the duty cycles of the two switches (the on-time of the switch referred to the period) d1, d2, one can write for the voltage-time balance across the main inductor:

$$U_1 d_1 = |U_1 - U_2|(1 - d_2) \tag{8}$$

The voltage transformation ratio is therefore:

$$M = \frac{U_2}{U_1} = \frac{1 + d_1 - d_2}{1 - d_2} \tag{9}$$

One can immediately see from Equation (9) that for a constant duty cycle of the second switch, the voltage transformation ratio is a linear function of the duty cycle of the first switch. **Figure 5a** shows the voltage transformation ratio with the duty cycle of switch S2 as a parameter and the duty cycle of switch S1 as a variable. The curve on the right side is the voltage transformation ratio of the original inverting Boost converter. **Figure 5b** shows the voltage transformation ratio when the duty cycle of the first switch is taken as a parameter and the duty cycle of the second switch is used as the independent variable. The derivative of the curves is reduced.



(a) **(b)**

Figure 5. Voltage transformation ratio: **(a)** Duty cycle of the second switch as parameter, and duty cycle of the first switch as variable; **(b)** duty cycle of the first switch as parameter, and duty cycle of the second switch as variable, remark: The semicolon at the duty cycle (x-axis) corresponds to the decimal point.

2.5. Simulation in the steady state

Figure 6 shows the input current, the current through the resonant inductor, the current through the main inductor, the input voltage, the control signal of the second switch, the control signal of the first switch, and the output voltage.

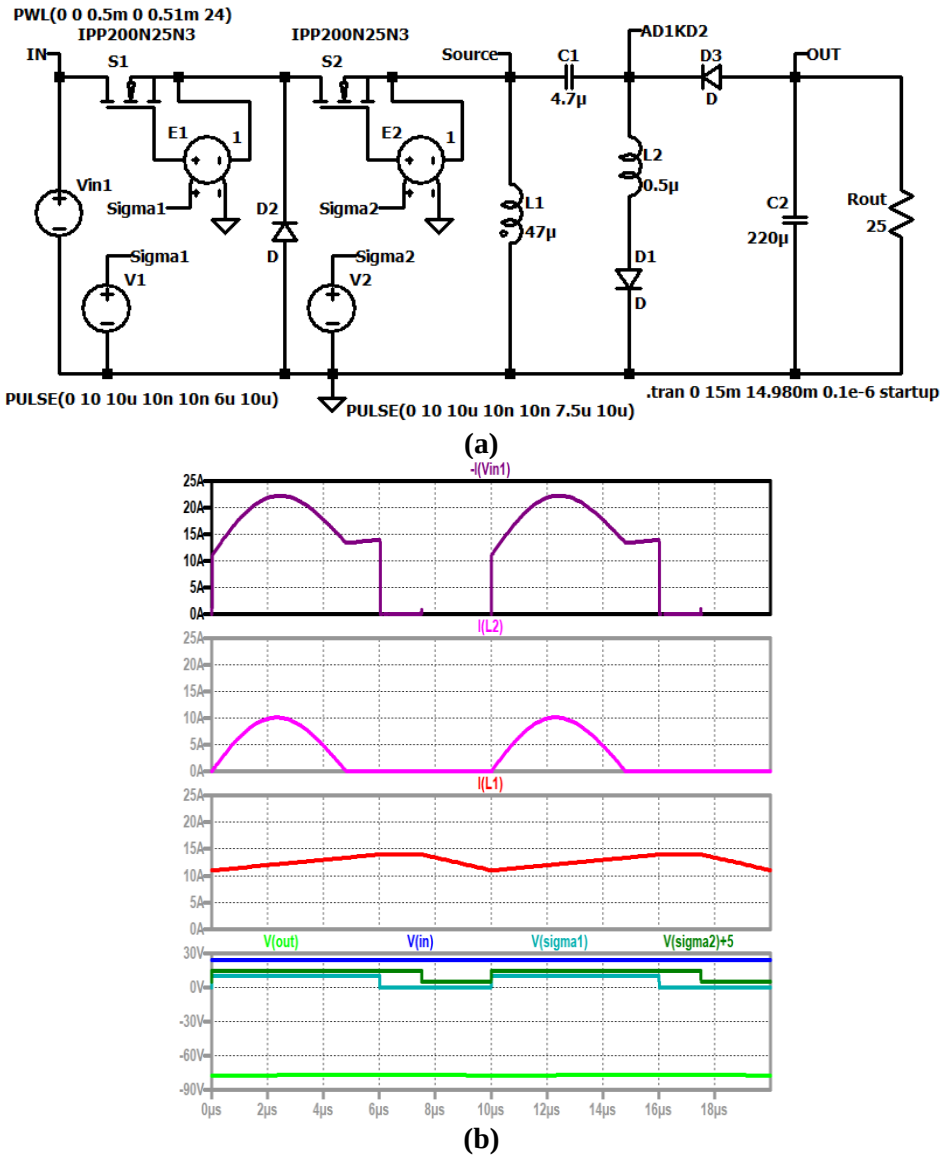


Figure 6. Steady state, **(a)** simulation circuit; **(b)** up to down: Input current (dark violet); current through the resonant inductor (violet); current through the main inductor (red); input voltage (blue), control signal of the second switch (dark green, shifted), control signal of the first switch (turquoise), output voltage (green).

2.6. Voltage stress

The voltage across the first switch is zero during M1, equal to the input voltage during M2 and stays at this value during M3.

The second switch is on during the first two modes and has to block the output voltage reduced by the voltage across C1 during M3 which is equal to the input voltage.

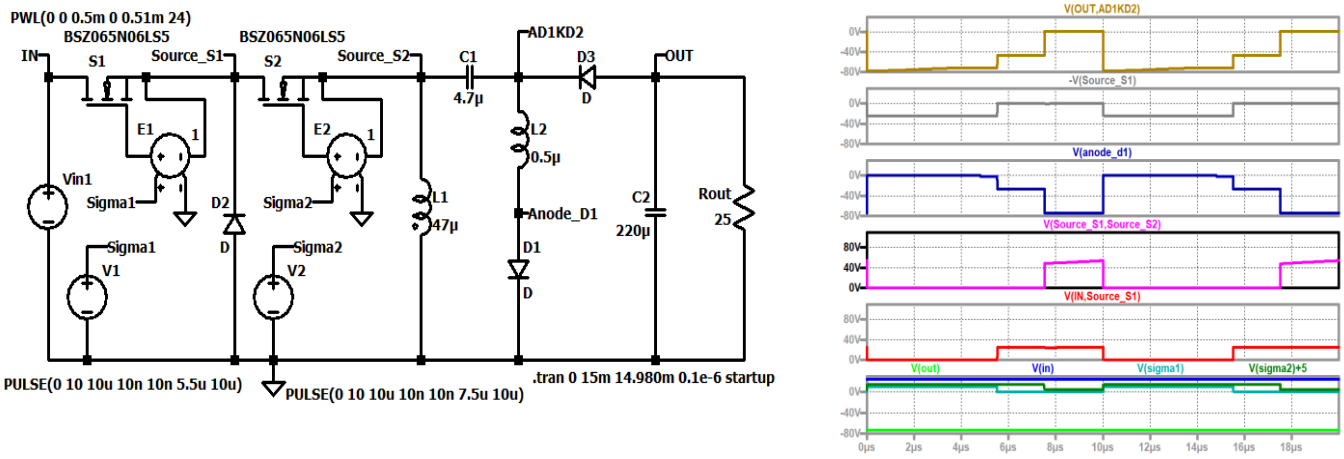
The diode D1 is on during the recharging process of C1 and the voltage across it stays at zero during the rest of mode M1. During mode M2, it has to block the voltage across C1 and during M3, it must block the output voltage.

The voltage across the tristate diode D2 is the negative input voltage during M1, the diode conducts during M2, and the voltage stays near zero during M3.

The free-wheeling diode D3 is stressed at M1 by the sum of the negative output and input voltages plus the voltage across C1. The voltage is reduced when the voltage across C1 is recharged. The voltage across the diode is approximately the output voltage. During mode M2, only the difference between the voltage across C1, which is equal to the input voltage, and the output voltage is across the diode. During M3 the diode is conducting.

Compared to the classical Boost converter, the voltage across the electronic switches is reduced. This may be an additional advantage of this topology.

Figure 7 shows the voltages across the semiconductor devices: The voltage across the free-wheeling diode D3, the voltage across the tristate diode D2, the voltage across the auxiliary diode D1, the voltage across the second switch S2, and the voltage across the first switch S1. Furthermore, one can see the input voltage, the control signals of the switches S2 and S1, and the output voltage.



(a) **(b)**

Figure 7. Voltages across the semiconductor devices, **(a)** simulation circuit; **(b)** up to down: Voltage across the free-wheeling diode D3 (brown); voltage across the tristate diode D2 (grey); voltage across the auxiliary diode D1 (dark violet); voltage across the second switch S2 (violet), voltage across the first switch S1 (red); input voltage (blue), control signal of switch S2 (dark green, shifted), control signal of switch S1 (turquoise), output voltage (green).

2.7. Current stress

In **Figure 8**, the currents through the semiconductor devices are shown: The current through the free-wheeling diode D3, the current through the tristate diode D2, the current through the auxiliary diode D1, the current through the second switch S2, and the current through the first switch S1. Additionally, the input voltage, the control signals of the electronic switches, and the output voltage are displayed.

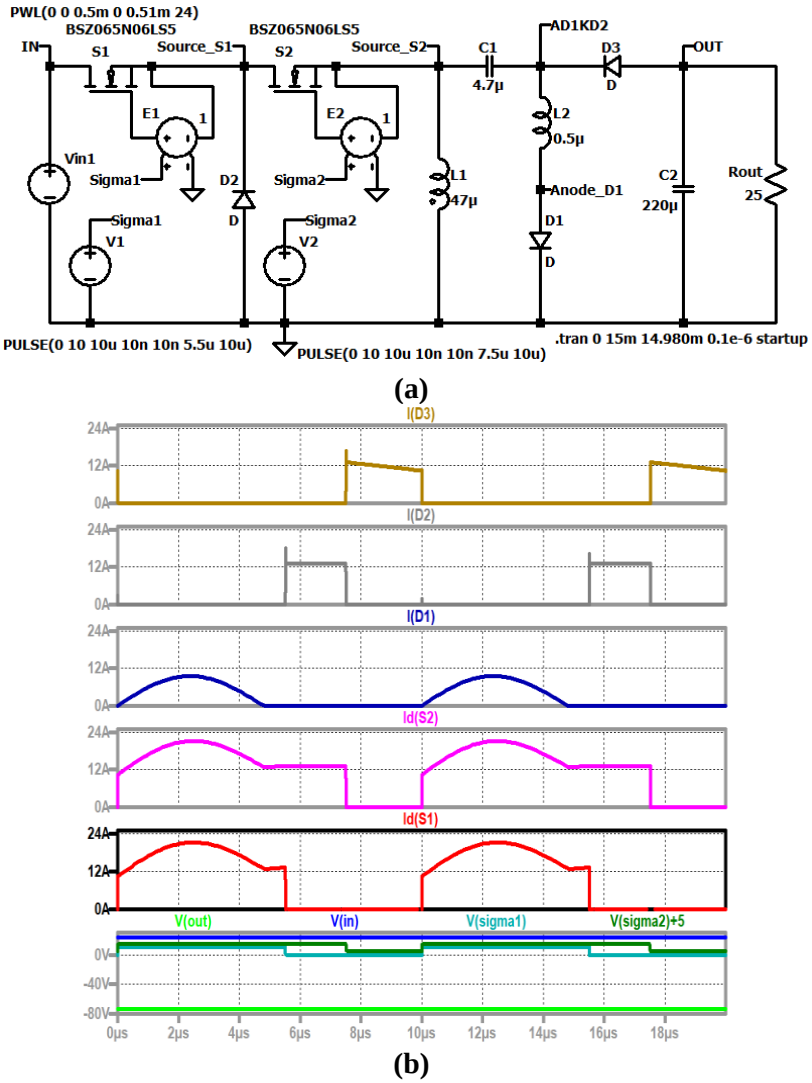


Figure 8. Currents through the semiconductor devices, **(a)** simulation circuit; **(b)** up to down: Current through the free-wheeling diode D3 (brown); current through the tristate diode D2 (grey); current through the auxiliary diode D1 (dark violet); current through the second switch S2 (violet), current through the first switch S1 (red); input voltage (blue), control signal of switch S2 (dark green, shifted), control signal of switch S1 (turquoise), output voltage (green).

3. Model of the tristate inverting boost converter

To study the dynamic behavior of the converter, the state space equations must be calculated. The capacitor C1 is charged to the input voltage at every period, and the current through L2 reaches zero. The converter can be studied as a second-order system with the state variables iL1 and uC2.

3.1. Idealized model

During the first mode, both electronic switches are on. The input voltage is across the main coil L1 and the output capacitor C2 supplies the load. Therefore, we get:

$$\frac{di_{L1}}{dt} = \frac{u_1}{L_1} \rightarrow \frac{du_{C2}}{dt} = \frac{-u_{C2}/R_1}{C_2} \tag{10}$$

During the second mode, when only the second switch is on, the coil L1 is short-circuited and the load is still supplied by the output capacitor:

$$\frac{di_{L1}}{dt} = \frac{"0"}{L_1} \rightarrow \frac{du_{C2}}{dt} = \frac{-u_{C2}/R_1}{C_2} \tag{11}$$

When the second electronic switch is turned off, the third mode starts. Now the difference between the voltage across C1 (which was charged to the input voltage) and the output voltage is across the coil; the current through the capacitor is the difference between the current through the coil and the current through the load. The mode M3 can be described by:

$$\frac{di_{L1}}{dt} = \frac{u_1 - u_{C2}}{L_1} \rightarrow \frac{du_{C1}}{dt} = \frac{i_{L1} - u_{C2}/R_1}{C_2} \tag{12}$$

To achieve the weighted model of the converter, the equations for mode M1 are multiplied by the duty cycle d1, for M2 by (d2−d1), and for M3 by (1−d2) and added. This leads to the large signal model of the converter according to:

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & \frac{d_2 - 1}{L_1} \\ \frac{1 - d_2}{C_2} & -\frac{1}{RC_2} \end{bmatrix}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1 + d_1 - d_2}{L_1} \\ 0 \end{bmatrix}(u_1) \tag{13}$$

This model is nonlinear. To use the Laplace transformation and to calculate the transfer functions, the model must be linearized around the operating point. The working point values are typified by capital letters with a zero in the index. The disturbances are marked by small letters with a roof on top. The products of the disturbances are deleted and so the linearization is achieved. The small signal model results in:

$$\frac{d}{dt}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & \frac{D_{20} - 1}{L_1} \\ \frac{1 - D_{20}}{C_2} & -\frac{1}{RC_2} \end{bmatrix}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix} + \begin{bmatrix} \frac{(1 + D_{10} - D_{20})}{L_1} & \frac{U_{10}}{L_1} & \frac{U_{C20} - U_{10}}{L_1} \\ 0 & 0 & -\frac{I_{L10}}{C_2} \end{bmatrix}\begin{pmatrix} \hat{u}_1 \\ \hat{d}_1 \\ \hat{d}_2 \end{pmatrix} \tag{14}$$

With abbreviations for the elements of the state matrix A and of the input matrix B, we get:

$$\frac{d}{dt}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix} + \begin{bmatrix} B_{11} & B_{12} & B_{13} \\ 0 & 0 & B_{23} \end{bmatrix}\begin{pmatrix} \hat{u}_1 \\ \hat{d}_1 \\ \hat{d}_2 \end{pmatrix} \tag{15}$$

Laplace transformation leads to:

$$\begin{bmatrix} s & -A_{12} \\ -A_{21} & s - A_{22} \end{bmatrix}\begin{pmatrix} I_{L1}(s) \\ U_{C2}(s) \end{pmatrix} = \begin{bmatrix} B_{11} & B_{12} & B_{13} \\ 0 & 0 & B_{23} \end{bmatrix}\begin{pmatrix} U_1(s) \\ D_1(s) \\ D_2(s) \end{pmatrix} \tag{16}$$

The denominator of all six transfer functions is given by the determinant of the coefficient matrix:

$$\text{Den} = s^2 - A_{22}s - A_{12}A_{21},\ \text{Den} = s^2 + \frac{1}{RC_2}s + \frac{(1-D_{20})^2}{C_2L_1} \tag{17}$$

The real part of the poles is at:

$$\delta = -\frac{1}{2RC_2} \tag{18}$$

The damping is larger for large loads (small resistors) and small output capacitors. The imaginary part is at:

$$\omega = \sqrt{\left|\frac{1}{(2RC_2)^2} - \frac{(1-D_{20})^2}{C_2L_1}\right|} \tag{19}$$

This shows the resonance angular frequency.

The most interesting transfer functions are the ones between the output voltage and the duty cycles because the control is done by the duty cycles.

For the numerator between the output voltage and the duty cycle of the first switch, one gets:

$$\text{Num\_}U_{C2}\text{to}D_1 = \begin{vmatrix} s & B_{12} \\ -A_{21} & 0 \end{vmatrix} = A_{21}B_{12} = \frac{1-D_{20}}{C_2} \times \frac{U_{10}}{L_1} \tag{20}$$

This result is very interesting. The transfer function has no zero; therefore, the converter is a phase-minimum system. The control is easier than that of the normal Boost converter.

When we look at the numerator concerning the duty cycle of the second switch:

$$\text{Num\_}U_{C2}\text{to}D_2 = \begin{vmatrix} s & B_{13} \\ -A_{21} & B_{23} \end{vmatrix} = -\frac{I_{L10}}{C_2}s + \frac{1-D_{20}}{C_2} \times \frac{U_{C20}-U_{10}}{L_1} \tag{21}$$

One sees that the term B23 is negative and therefore the zero is on the right side of the complex plane. The circuit is now a non-phase-minimum system, and the zero shifts the phase by an additional −90°. The position of the zero is at:

$$s_Z = +\frac{1-D_{20}}{L_1} \times \frac{U_{C20}-U_{10}}{I_{L10}} \tag{22}$$

It depends on the operating point and the main inductor. The smaller the value of the coil, the farther to the right the zero is shifted and the more unimportant its influence is.

The two poles each also shift the phase by −90°. The controlled system is slower because the cut-through frequency must be shifted more to the left (to lower frequencies). To control the system, it is therefore better to leave the duty cycle of the second switch constant and to control the system by the duty cycle of the first switch.

It should be mentioned that converters with step-up behavior are normally non-phase-minimum systems. Another possibility to improve the dynamics of the converter is to use a feed-forward control.

The numerator describing the influence of the input voltage can be found by:

$$\text{Num\_}U_{C2}\text{to}U_1 = \begin{vmatrix} s & B_{11} \\ -A_{21} & 0 \end{vmatrix} = +A_{21}B_{11} = \frac{1-D_{20}}{C_2} \times \frac{(1+D_{10}-D_{20})}{L_1} \quad (23)$$

This leads again to a phase-minimum system.

For the operating point one gets by linearization of Equation (15):

$$(D_{20}-1)U_{C20} + (1+D_{10}-D_{20})U_{10} = 0,\ (1-D_{20})I_{L10} - \frac{U_{C20}}{R} = 0 \quad (24)$$

This leads to the voltage transformation ratio:

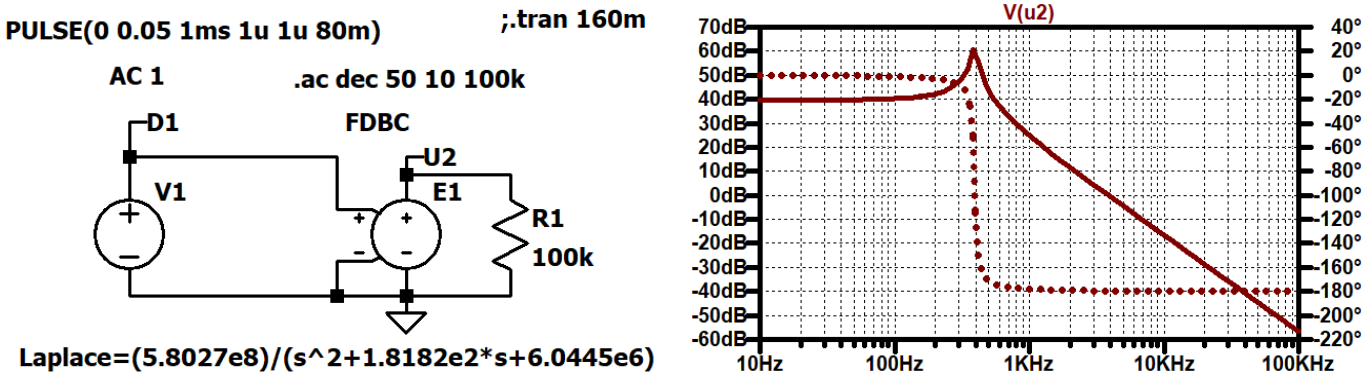
$$\frac{U_{20}}{U_{10}} = \frac{U_{C20}}{U_{10}} = \frac{1+D_{10}-D_{20}}{1-D_{20}} \quad (25)$$

The connection between the current through the main coil and the load current is:

$$I_{L10} = \frac{U_{C20}}{R(1-D_{20})} = \frac{I_{LOAD0}}{1-D_{20}} \quad (26)$$

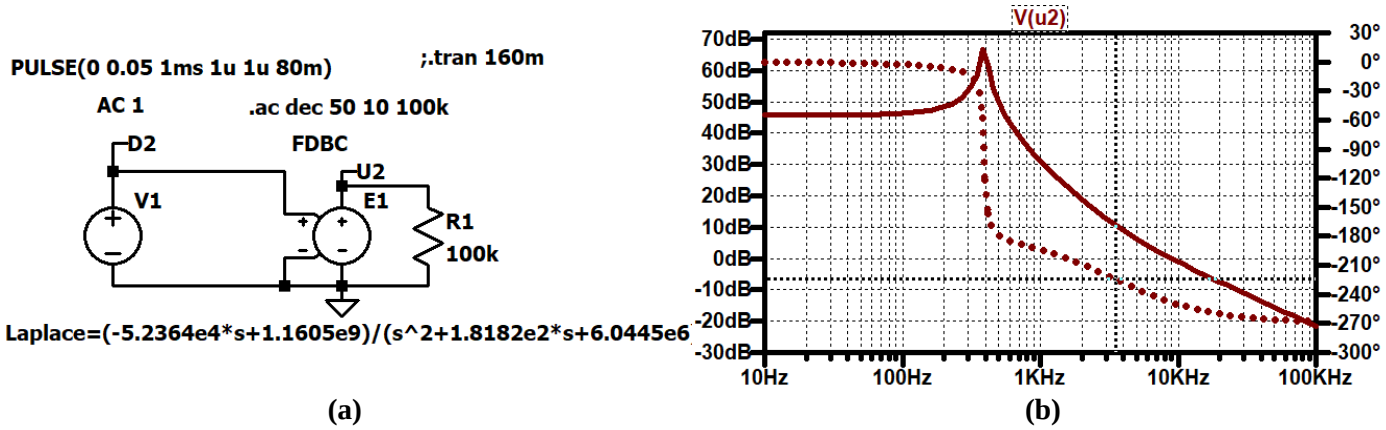
The Bode plots are shown for L1 = 47 µH, C2 = 220 µF and the working point U10 = 24 V, D10 = 0.5, D20 = 0.75, R = 25 Ω. The resonant frequency caused by the poles is at 390 Hz and can be seen in all Bode plots.

Figure 9 depicts the Bode plot between the output voltage and the duty cycle of switch S1. **Figure 10** displays the Bode plot between the output voltage and the duty cycle of switch S2. The zero on the right side shifts the phase to −270°. The frequency of the zero is about 3.6 kHz which is about a decade higher than the frequency of the poles.



(a) **(b)**

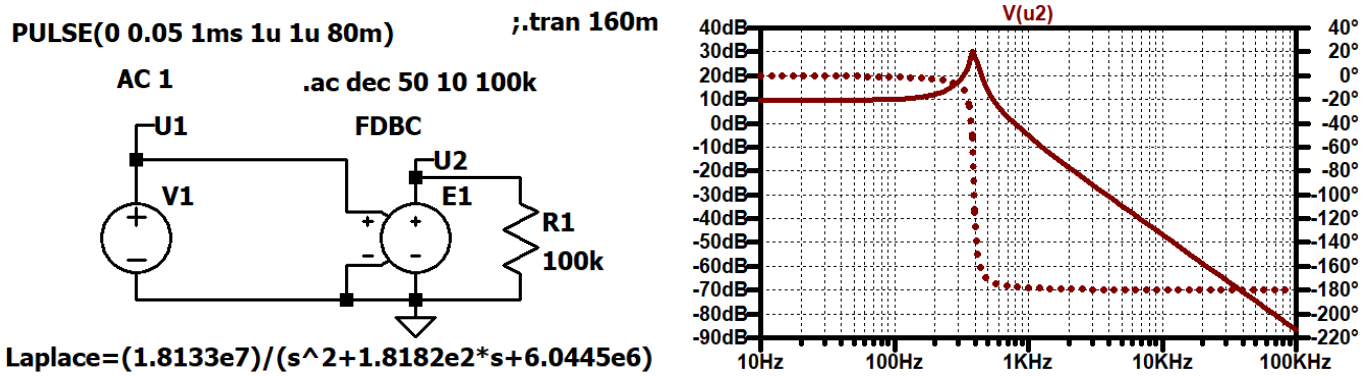
Figure 9. Bode plot output voltage referred to the duty cycle of switch S1, **(a)** simulation circuit; **(b)** solid line: Gain, dotted line: Phase.



(a) **(b)**

Figure 10. Bode plot output voltage referred to the duty cycle of switch S2, **(a)** simulation circuit; **(b)** gain: Solid line, phase: Dotted line.

Figure 11 shows the Bode plot between the output voltage and the input voltage.



(a) **(b)**

Figure 11. Bode plot output voltage referred to the input voltage, **(a)** simulation circuit; **(b)** gain: Solid line, phase: Dotted line.

Figure 12 shows the implementation of this model with LTSpice and the duty cycles d1 and d2, the current through the main coil and the output voltage. The start-up is done by a ramp of the duty cycles. Steps of the duty cycle lead to a pronounced ringing. This is caused by the idealized modeling.

The depicted Bode plots are for one operating point and nominal values of the components. For the design of the controller, more plots are necessary showing the tolerances of the components and maximum and minimum operating points. The design of the controller will be done so that a stable controlled system is achieved for all these cases.

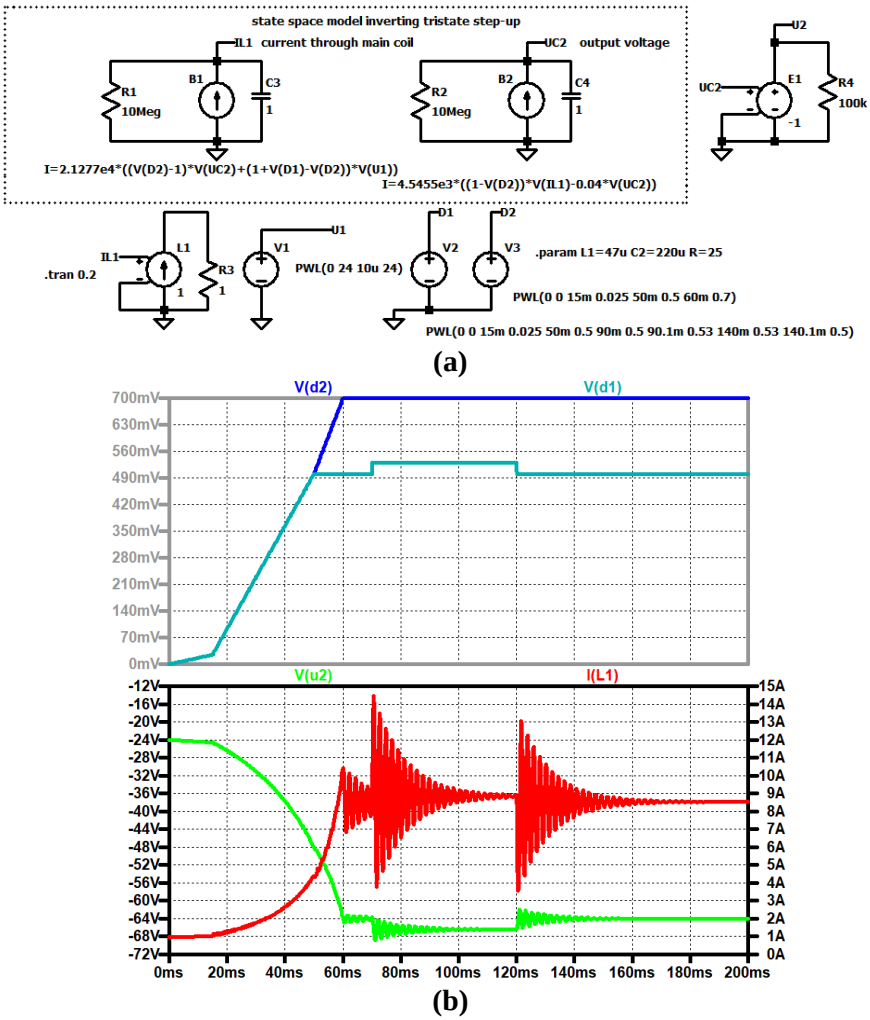


Figure 12. Idealized model, start-up and duty cycle steps, **(a)** simulation circuit and **(b)** up to down: Duty cycle of switch two (blue), duty cycle of switch one (turquoise), current through L1 (red), output voltage (green).

3.2. Model with parasitic resistors

To get a more precise model, one must include the parasitic resistors in the calculation. In each period, the capacitor C1 is charged up to the input voltage, and the current through the inductor L2 must be zero at the end of mode M1. So the current through the auxiliary inductor L2 and the voltage across the intermediate capacitor C1 are not state variables for describing the dynamics of the converter. Only the current through the main inductor L1 and the voltage across the output capacitor C2 are necessary for describing the converter.

3.2.1. M1: Both active switches are on

Figure 13 shows the equivalent circuit during mode M1.

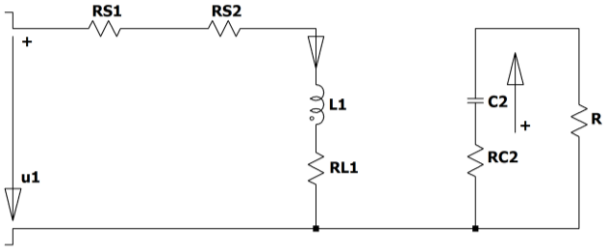


Figure 13. Equivalent circuit during M1.

The state equations are:

$$\frac{di_{L1}}{dt} = -\frac{(R_{L1}+R_{S1}+R_{S2})i_{L1}+u_1}{L_1}, \frac{du_{C2}}{dt} = -\frac{u_{C2}}{C_2(R+R_{C2})} \tag{27}$$

3.2.2. M2: S1 is off and D2 is on

The equivalent circuit is shown in **Figure 14**. The tristate diode D2 is modeled by the knee voltage VD and the resistor RD. This leads to the state equations:

$$\frac{di_{L1}}{dt} = -\frac{(R_D+R_{L1}+R_{S2})i_{L1}-V_D}{L_1}, \frac{du_{C2}}{dt} = -\frac{u_{C2}}{C_2(R+R_{C2})} \tag{28}$$

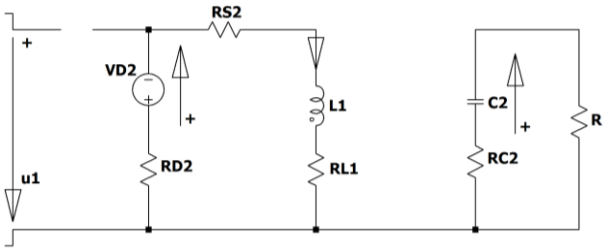


Figure 14. Equivalent circuit during M2.

3.2.3. M3: The free-wheeling diode D3 is conducting

The equivalent circuit is depicted in **Figure 15**. The capacitor C1 is modeled in this case by the input voltage and the parasitic series resistor. With Kirchhoff's current law (KCL), one can write for the output node:

$$i_{L1} = i_{C2} + \frac{u_{C2} + R_{C2}i_{C2}}{R} \tag{29}$$

From this equation one gets the current through the output capacitor C2. For reduced writing we use the abbreviation

$$R//R_{C2} = \frac{RR_{C2}}{R + R_{C2}} \tag{30}$$

Now one gets the state equations of the current through the main coil:

$$\frac{di_{L1}}{dt} = \frac{1}{L_1}\left\{-(R//R_{C2} + R_{C1} + R_D + R_{L1})i_{L1} - \frac{R}{R + R_{C2}}u_{C2} + u_1 - V_D\right\} \tag{31}$$

For the voltage across the output capacitor one gets:

$$\frac{du_{C2}}{dt} = \frac{Ri_{L1} - u_{C2}}{C_2(R + R_{C2})} \tag{32}$$

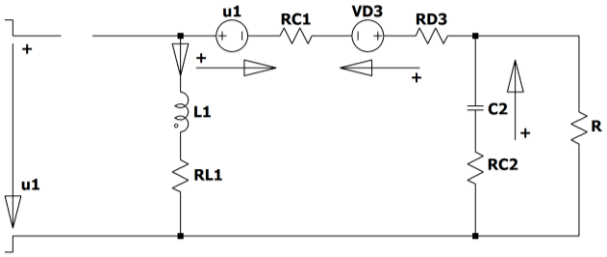


Figure 15. Equivalent circuit during M3.

3.2.4. Large signal model

To obtain the large signal model of the converter, one has to weight the state equations of mode M1 by the duty cycle of switch S1 d1, the equations of M2 by (d2−d1), and the state equations of mode M3 by (1−d2), leading to:

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} -\dfrac{R_{L1} + R_{S1}d_1 + R_{S2}d_2 + (R_{C1} + R_D)(1 - d_1) + R//R_{C2}(1 - d_2)}{L_1} & \dfrac{(d_2 - 1)}{L_1(R + R_{C2})} \\ \dfrac{(1 - d_2)R}{C_2(R + R_{C2})} & -\dfrac{1}{C_2(R + R_{C2})} \end{bmatrix} \times \\ \times \begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \dfrac{1 - d_2 + d_1}{L_1} \\ 0 \end{bmatrix} (u_1) + \begin{pmatrix} \dfrac{(d_1 - 1)V_D}{L_1} \\ 0 \end{pmatrix} \quad (33)$$

The knee voltage of both diodes is set equal.

Figure 16 shows the LTSpice implementation of the model with parasitic resistors. The derivatives are written as controlled current sources and the integration is done by capacitors of 1 F; the 10 MΩ resistors are only for stabilization. With the voltage-controlled voltage source E1, the output voltage is calculated from the state variable uC2. The voltage-controlled current source B1 is used to get a current for the figure (the integrated values are voltages).

Figure 17 depicts the simulation circuit of the converter with pulse width modulation (PWM). The comparators U1 and U2 serve as PWM-modulators. The carrier signal is a triangle with the frequency of 100 kHz. In **Figure 18**, the simulation of the circuit and of the model are given. The model with the resistors is very fast and shows the dynamics of the mean values. Compared to the idealized model, it describes the circuit very precisely. The circuit simulation takes more than a hundred times longer and shows the current ripple. For the checking of controllers, the model simulation is sufficient. Only in a last step can the circuit-oriented model be used. The model is valid when the output voltage is greater than or equal to the input voltage.

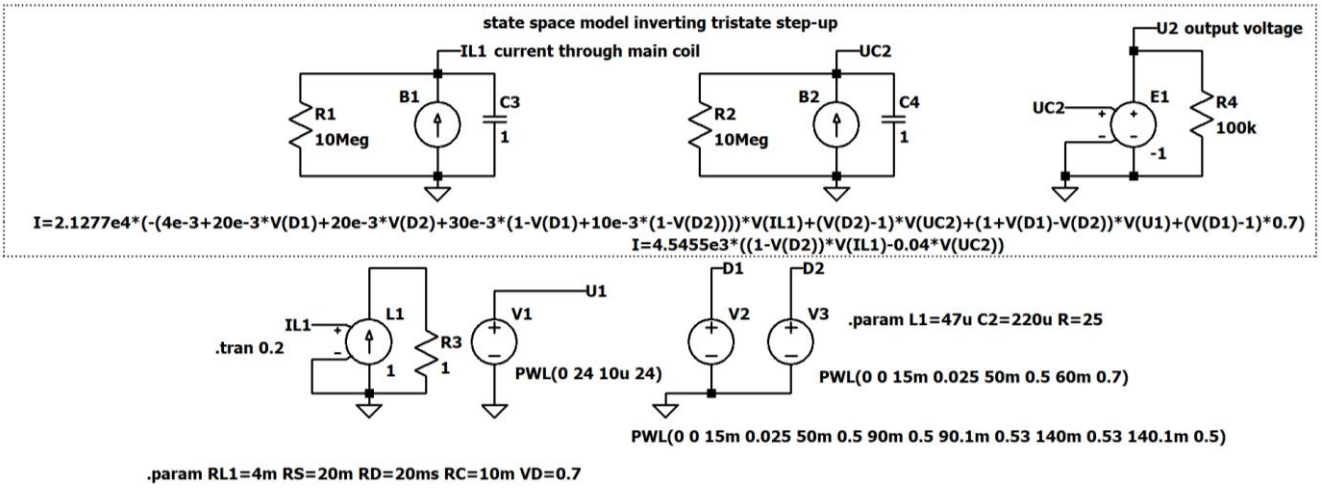


Figure 16. LTSpice implementation of the model with parasitic resistors.

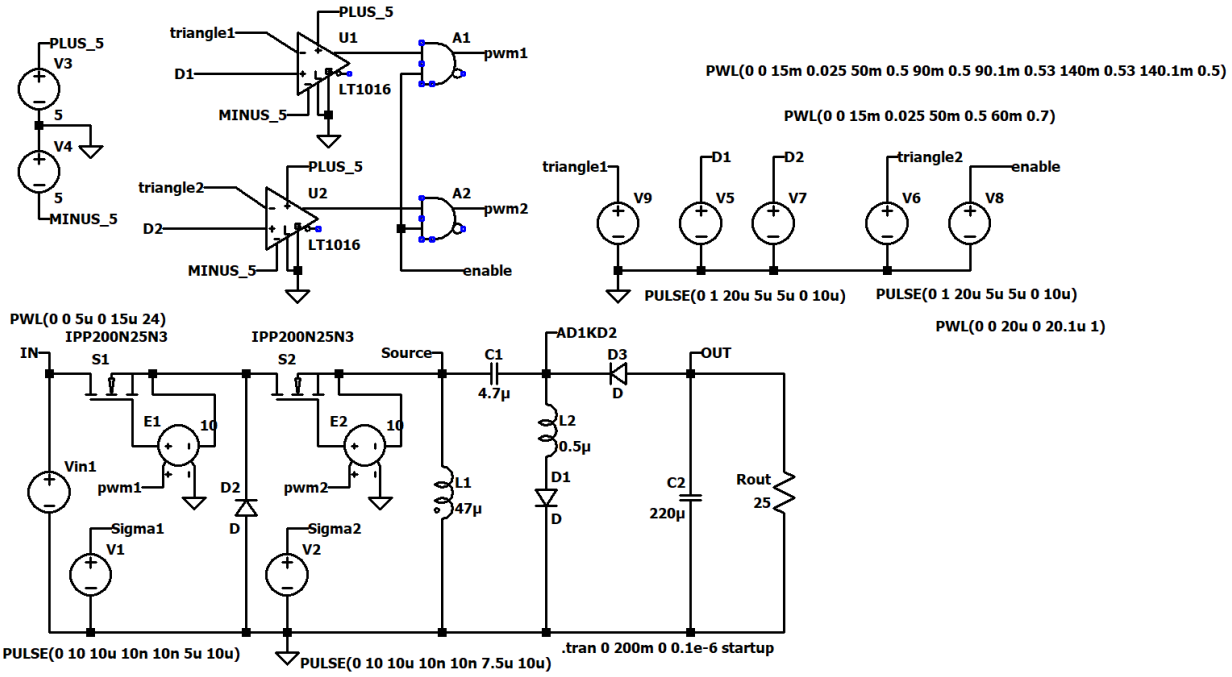


Figure 17. Simulation circuit.

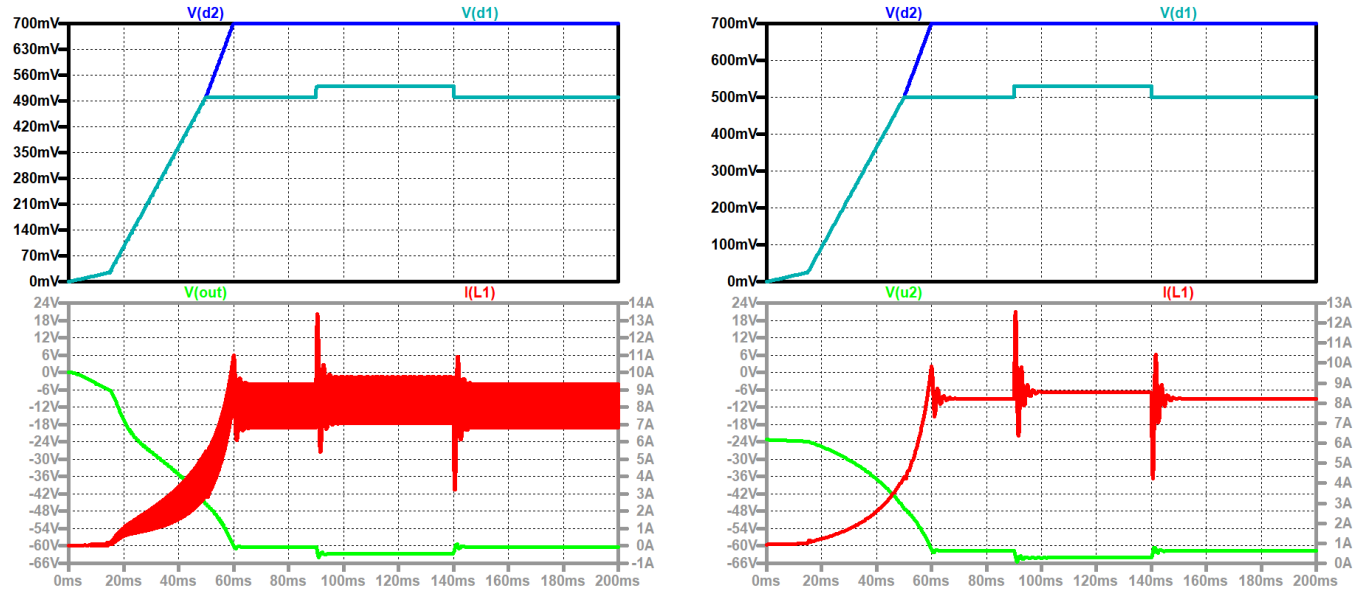


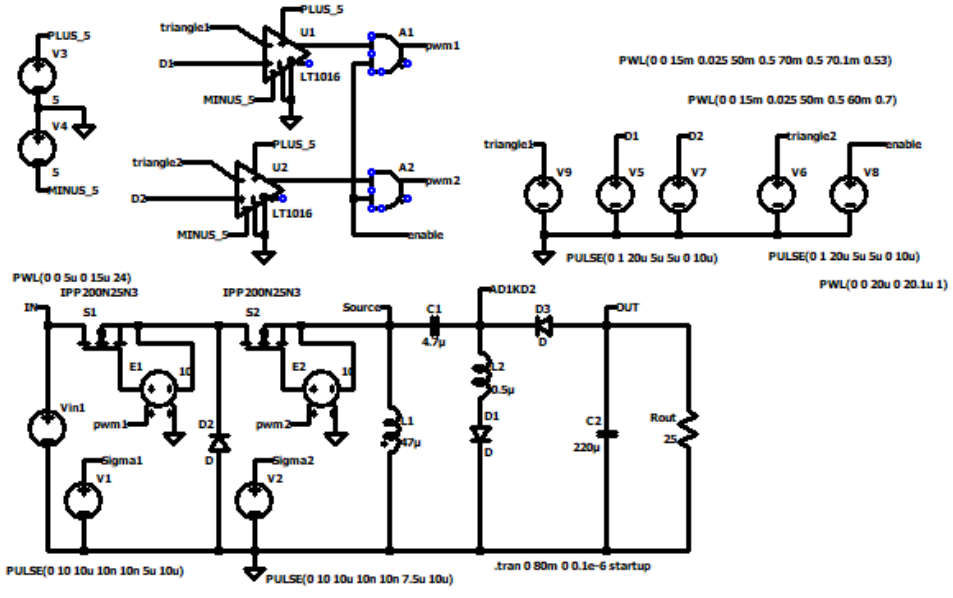
Figure 18. Start-up and duty cycle steps, up to down: Duty cycle of switch S2 (blue), duty cycle of switch S1 (turquoise), current through the main coil (red), output voltage (green): **(a)** Simulation with the circuit according to **Figure 17**; **(b)** simulation with the model according to **Figure 16**.

3.3. Start-up

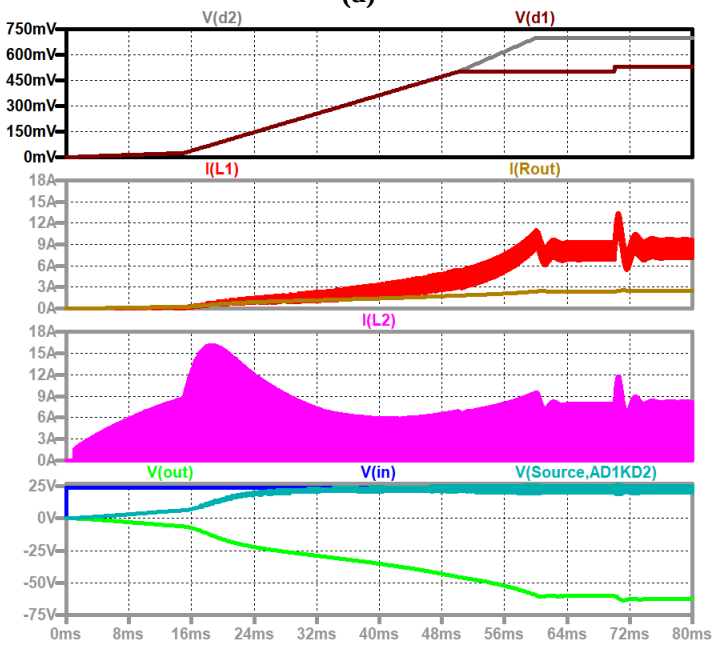
The position of the electronic switches is on the high side, and they are in series to the input source. So no inrush occurs when the converter is directly connected to a stable input source. Furthermore, the switches (especially S1) can be used as an electronic fuse in case of an error.

The start-up begins with ramp functions for the duty cycles. The slower the increase, the smaller the current through the auxiliary coil. After 50 ms the operating point of the first switch is reached and 10 ms later the operating point of the second switch is obtained. The duty cycle of S2 is now constant and the converter is controlled by switch S1. The step response of a duty cycle step at 70 ms can be seen.

During the start-up, the on-time of the switches is so short that a half-wave through L2 can occur. When S1 turns off and S2 is still on, the current will free-wheel over S2, and when both switches are off, the current through L2 can flow through D2 and charge the output capacitor. **Figure 19** shows the duty cycle of S2, the duty cycle of S1, the current through the main coil, the load current, the current through the auxiliary coil, the input voltage, the voltage across the intermediate capacitor, and the output voltage.



(a)



(b)

Figure 19. Start-up, **(a)** simulation circuit; **(b)** up to down: Duty cycle of S2 (grey), duty cycle of S1 (black); current through the main coil (red), load current (brown); current through the auxiliary coil (violet); input voltage (blue), voltage across the intermediate capacitor (turquoise), output voltage (green).

4. Dimensioning hints

The dimensioning is sketched for operation in the linearized voltage transformation mode. Starting from the desired minimum and maximum input and output voltages and with **Figure 5a**, the duty cycle d2, and the minimum and maximum duty cycles d1 are chosen. With the maximum load current, a chosen maximum voltage ripple Δu_{C2}, and a switching period T, one gets for the output capacitor:

$$C_2 > I_{LOAD} \frac{d_{2\max} T}{\Delta u_{C2}} \tag{34}$$

This value does not take the voltage drop $R_{C2} I_{Load}$ into account. The capacitor must be larger.

The current through L1 rises during M1 by ΔI_{L1}. This leads to:

$$L_1 = \frac{U_1 d_{1\max} T}{\Delta I_{L1}} \tag{35}$$

The mean value of the inductor current during the modes M1 and M3 $\bar{I}_{L1,M1M3}$ can be used to get a connection with the load current which can be taken as constant. The charge balance across C2 can be written according to:

$$I_{LOAD} \times d_2 T = \left[\bar{I}_{L1,M1M3} - I_{LOAD}\right](1 - d_2)T \tag{36}$$

This leads to the connection:

$$\bar{I}_{L1,M1M3} = \frac{I_{LOAD}}{1 - d_2} \tag{37}$$

The current through L1 starts at $\bar{I}_{L1,M1M3} - \frac{\Delta I_{L1}}{2}$ and ends at $\bar{I}_{L1,M1M3} + \frac{\Delta I_{L1}}{2}$, when switch S1 is turned off. It stays constant during M2 and reaches $\bar{I}_{L1,M1M3} - \frac{\Delta I_{L1}}{2}$ again at the end of M3. During M3 the capacitor C1 is discharged according to:

$$\Delta u_{C1} = \frac{1}{C_1} \int_{d_2 T}^{T} \bar{I}_{L1,M1M3} dt = \frac{1}{C_1} \bar{I}_{L1,M1M3} (1 - d_2) T \tag{38}$$

This leads to a capacitor value of:

$$C_1 > \frac{I_{LOAD} T}{\Delta u_{C1}} \tag{39}$$

From Equation (5), L2 can be determined with the help of the inequality:

$$T_{on,\min}^2 = \left(d_{1,\min} T\right)^2 > \pi^2 C_1 L_2 \tag{40}$$

One gets for the value of the inductor L2:

$$L_2 < \frac{T_{on,\min}^2}{\pi^2 C_1} = \frac{\left(d_{1,\min} T\right)^2}{\pi^2 C_1} \tag{41}$$

With Equation (6), the peak current of the resonant circuit can be obtained. There the value ΔuC1 is half of the complete change of the voltage. Considerations concerning the dynamics can be found in Section 3.1.

5. Conclusion

A converter that produces a higher negative output voltage compared to the input voltage was presented here. The converter has interesting features. It is a tristate converter, which means there are two electronic switches to control it. When the duty cycle of the second switch is larger than that of the first switch and is held constant,

the converter can be controlled by changing the duty cycle of the first switch. Controlling in this way linearizes the voltage transformation ratio and the system has a phase-minimum behavior. Holding the duty cycle of the first switch constant and making the control by changing the duty cycle of the second switch leads to a non-phase-minimum system and to a non-linear voltage transformation ratio. Another interesting aspect is the fact that the voltage stress of the electronic switches is reduced compared to that of the classical Boost converter. No inrush current occurs when the converter is connected to a stable supply. The switches of the converter can also be used as an electronic fuse.

Conflict of interest: The author declares no conflict of interest.

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