Universe Scientific Publishing

Clean Energy Science and Technology 2024, 2(4), 263.
https://doi.org/10.18686/cest263

Article

Research progress of low-temperature plasma polishing technology in chip material processing

Hui Yan[†], **Shuang Xue**[†], **Peiwen Guo**[†], **Jiale He**, **Guangning Wang**, **Yinlong Zeng**, **Longfei Qie**, **Ruixue Wang**[*]

Beijing University of Chemical Technology, Beijing 100029, China
* **Corresponding author:** Ruixue Wang, wrx@mail.buct.edu.cn
† Hui Yan, Shuang Xue, and Peiwen Guo contributed equally to this article.

CITATION

Yan H, Xue S, Guo P, et al. Research progress of low-temperature-plasma polishing technology in chip material processing. Clean Energy Science and Technology. 2024; 2(4): 263. https://doi.org/10.18686/cest263

ARTICLE INFO

Received: 5 September 2024
Accepted: 6 November 2024
Available online: 21 November 2024

Abstract: Low-temperature plasma polishing technology, by virtue of the plasma's highly ionized characteristics, can accurately remove tiny defects and impurities on the surface of chip materials, improve the flatness and finish of chip materials, reduce mechanical damage and subsurface damage, and has a high material removal rate. This paper reviews the application status, advantages and limitations of plasma polishing technologies in the field of chip material processing. The principles and applications of plasma-assisted polishing, plasma chemical vaporization machining, plasma electrolytic processing-mechanical polishing and plasma assisted selective etching are specifically discussed, and their advantages and limitations are analyzed. Finally, the development of plasma chip-polishing technology is prospected, aiming to provide a useful reference for the continuous improvement of chip manufacturing processes and the future development of the microelectronics industry.

Keywords: low-temperature plasma polishing; plasma-assisted polishing (PAP); plasma electrolytic processing-mechanical polishing (PEP-MP); plasma chemical vaporization machining (PCVM); plasma assisted selective etching (PASE)

1. Introduction

As a core component of modern science and technology, chips have ideal characteristics, such as high integration, high reliability, high speed and low power consumption. With their excellent performance and continuously improved manufacturing process, they play a vital role in the energy field. For example, in solar cells, chip technology is used for power conversion, which greatly improves the efficiency of photoelectric conversion [1]. In smart grids, chips are used for power storage and regulation, realizing efficient management and optimization of power systems [2]. In renewable energy systems, chips are used in battery management systems to ensure the safety and efficient use of batteries [3,4]. In addition, chips also support energy collection and energy management systems, improving energy utilization and stability. In recent years, chips help to promote the development of the clean energy field and provide strong support for achieving the goal of sustainable development.

Chip materials are raw materials that constitute the basic structure of the entire semiconductor chip. They need to be prepared into high-quality wafers to achieve the key role of fixing and carrying [5]. With the increase in application demand and the continuous development of science and technology, chip materials are also continuously improved and innovated [6]. The development of chip materials has gone through the following stages: the first generation is single-element semiconductors represented by silicon and germanium. Silicon-based semiconductors are widely used in computers and other electronic products due to their excellent semiconductor properties, high stability, high yield, low cost and mature processing technology. The second generation is III-V compound semiconductors represented by gallium arsenide (GaAs). Due to their high electron mobility and excellent optoelectronic properties, they are suitable for 5G communications and optoelectronic devices (such as LEDs, lasers, etc.). The third generation is wide-bandgap semiconductors represented by gallium nitride (GaN) and silicon carbide (SiC) [7–9], which have a high breakdown voltage, high thermal conductivity and other characteristics, and are suitable for radio frequency (RF) devices in high-power and high-temperature environments [10–12]. The fourth generation is ultra-wide bandgap materials represented by diamond and aluminum nitride and ultra-narrow bandgap materials represented by gallium antimonide (GaSb). With their extremely high hardness and thermal conductivity, they have good stability and durability in environments with high heat and high pressure. From the initial chip raw materials to the final chip products, there are four process flows: chip design, wafer production, chip packaging and chip testing. As chip size continues to shrink and integration increases, the functions and circuits contained in the chip become more complex, which puts more stringent requirements on its preparation process [13–15]. During the wafer production process, multiple process steps need to be precisely controlled, such as lithography, etching, polishing, doping and thin film deposition, and these processes must be performed at micron or even nanometer precision, which places extremely high demands on the surface quality of the wafer bare die [16,17]. However, surface defects and roughness naturally form during the wafer bare die production process and limit the further improvement of chip performance. The wafer bare die preparation process mainly includes several key steps: ingot growth, slicing, grinding, polishing and packaging [18], as shown in **Figure 1**. First, a raw material is synthesized and grown into ingots at a high temperature, which are then sliced and thinned by wire cutting. The marks and defects left by cutting and other surface wear are then removed by grinding, and the internal stress introduced during the slicing process is eliminated. Subsequently, the ingots are polished to a high-quality surface state to ensure that there is no excess material or defects on the surface of the wafer. Finally, they are vacuum-sealed and transported to subsequent process scenarios. Among them, the polishing process can effectively remove undesirable oxides and impurities on the surface, significantly reduce defects on the wafer's surface and achieve high-precision flatness and finish on the chip's surface, thereby improving the yield and device performance of the entire manufacturing process. Problems such as material selectivity, surface damage and polishing rate are often encountered during the polishing process. Therefore, the development of efficient polishing technology has attracted much attention.

Low-temperature plasma is generated by gas ionization in the discharge space, and a large number of active particles are generated through a series of physical and chemical processes. Its unique properties make it extremely active at the microscopic scale, laying the foundation for the application of plasma in the field of chip polishing [19,20]. Low-temperature plasma polishing technology uses these active particles to undergo physical and chemical reactions with the surface of the chip material. High-speed electrons can excite, ionize or break reaction molecules into free radical fragments. Ions and certain neutral atoms etch a substrate's surface, and some neutral atoms react chemically with free radicals on the surface of the substrate to form a softening layer, which provides conditions for subsequent mechanical polishing. Through plasma polishing, tiny defects and impurities can be removed to achieve fine processing of a chip's surface, thereby improving the surface quality and performance of the chip [21].

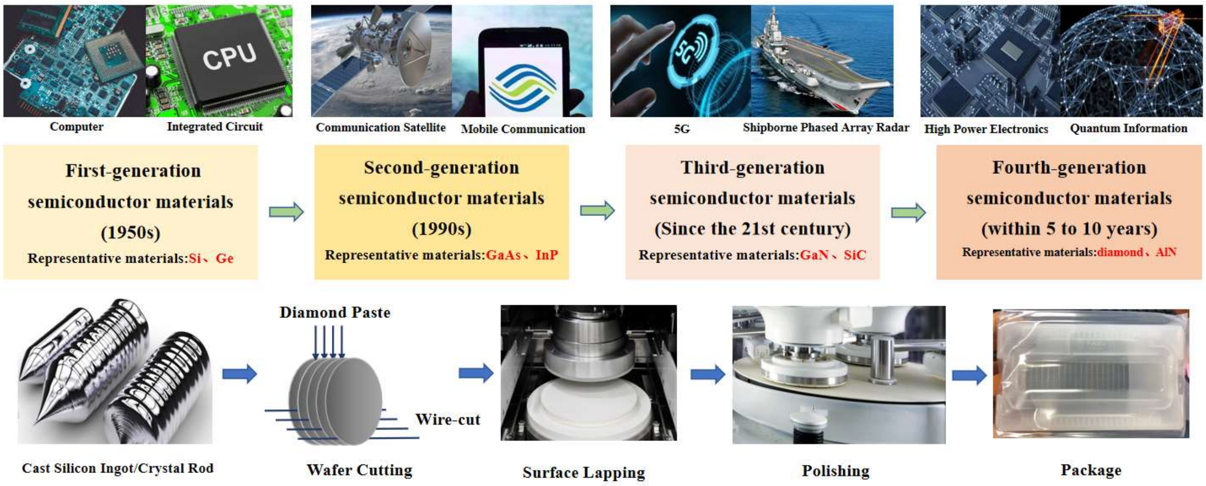

Figure 1. Chip applications, material development and wafer preparation process.

Low-temperature plasma polishing technology can not only remove nanoscale defects and impurities by selectively etching a wafer's surface, making the chip's surface smoother and flatter, but also significantly improve polishing efficiency and reduce processing time, thus improving production efficiency. Compared with traditional mechanical polishing, low-temperature plasma polishing causes less damage to the subsurface of the chip, helping to improve the overall performance and reliability of the chip. In addition, plasma technology can precisely control the nanometer-scale roughness of the chip's surface, which is crucial for improving the integration of microelectronic devices. As a green and clean processing method, low-temperature plasma polishing does not require the use of a large number of chemical reagents, reduces the generation of harmful waste, and is environmentally friendly. Although low-temperature plasma polishing technology has achieved remarkable results, there are still some challenges, such as the complexity of precise control of plasma processing machine tools and the synergistic improvement of the polishing rate and quality. Therefore, in-depth research and technological innovation on low-temperature plasma polishing technology are not only related to the optimization of existing chip manufacturing processes but also propose new research topics for future microelectronic device manufacturing.

Low-temperature plasma polishing technology has become an important research direction in materials science and microelectronics manufacturing in the field of chip material processing. Many researchers have conducted in-depth discussions on it and published relevant review articles. Li et al. [22] introduced in detail several polishing methods for single-crystal diamond, mainly direct and assisted polishing technologies based on various energy beams, such as laser polishing, ion beam polishing, and plasma-assisted polishing and laser-assisted polishing, and highlighted the characteristics and application scope of different methods. Geng et al. [23] reviewed atomic-scale and near-atomic-scale polishing methods on flat and curved surfaces, including chemical mechanical polishing, plasma-assisted polishing, catalyst reference etching, valve cover polishing, elastic emission machining, ion beam shaping, magnetorheological polishing and fluid jet polishing, discussed in detail in terms of removal mechanisms, polishing systems and industrial applications. It can be seen that existing reviews extensively covered various chip material polishing technologies and discussed different technology types but did not deeply explore the specific process principles and application scenarios of plasma-related technologies. Furthermore, there was less emphasis on the analysis of process details and more on the breadth and development trends of technology. In addition, existing reviews only analyzed the effect of polishing technology in a single material, lacking systematic comparisons of other chip materials.

From the perspective of various chip materials, this article mainly introduces the application research progress of low-temperature plasma technologies in the field of chip polishing, focusing on four low-temperature plasma polishing processes, and reviews in detail the principles of different processes and their application in different chip materials. Applications in plasma-polishing chips are analyzed and discussed, and its advantages and existing limitations, are analyzed and discussed. Finally, the development of the plasma polishing of chips is prospected. Compared with a review that more broadly covers polishing technologies, this article helps readers understand the advantages, disadvantages and control methods of these technologies in practical applications by detailing key properties, such as the material removal rate and surface roughness from each process. Four representative plasma polishing technologies covering mainstream chip manufacturing needs were selected, demonstrating their applicability to a variety of materials, such as silicon, silicon carbide, gallium nitride and single-crystal diamond, and not only for multi-materials. The comprehensive analysis of multiple processes lays a solid foundation and provides a useful reference for the continuous improvement of chip manufacturing processes and the future development of the microelectronics industry.

2. Chip polishing technologies

2.1. Traditional polishing technologies

With the continuous development of semiconductor technology, chip polishing technology has also undergone a variety of process evolution and innovation. Traditional chip polishing processes include mechanical polishing (MP), chemical mechanical polishing (CMP), ultrasonic-vibration-assisted polishing (UVAP), electrochemical-assisted polishing (ECAP), magnetorheological finishing (MRF), photocatalytic mechanical polishing (PCMP) and ion beam polishing (IBP), as shown in **Figure 2**. MP technology was born in the late 19th century and was widely used in the early 20th century. It was first used for the surface treatment of optical and metal materials and then gradually applied to the field of chip manufacturing. As the earliest polishing technology used in chip manufacturing, the basic principle of MP technology is to grind a wafer's surface with mechanical force and abrasives to remove surface roughness and defects [24,25]. Mechanical polishing has the advantages of simple operation and low cost but it also has problems, such as easy to cause stress damage on the wafer's surface and poor material selectivity, and so it was gradually replaced by more advanced technologies. CMP technology was invented in the early 1950s and entered the semiconductor manufacturing process in the 1980s, becoming one of the key planarization technologies in integrated circuit manufacturing. CMP technology combines mechanical grinding and chemical reactions on the basis of mechanical polishing. The chemical components in the polishing liquid (such as hydrofluoric acid, hydrogen peroxide, etc.) react chemically with a wafer's surface to generate an easily removable soft layer [26,27]. At the same time, a polishing pad contacts the softened surface under a certain pressure value and mechanically grinds the surface under the action of rotation or reciprocating motion. Through the synergistic effect of chemistry and mechanics, the flattening and the high-precision polishing of a material's surface are achieved [28,29]. CMP technology excels in improving polishing accuracy and reducing surface damage. It can achieve a high material removal rate (MRR of 500–5000 nm/h), low surface roughness (R_a of 0.5–2 nm) and good processing uniformity (uniformity of ±2–5%), and it is widely used in modern chip manufacturing.

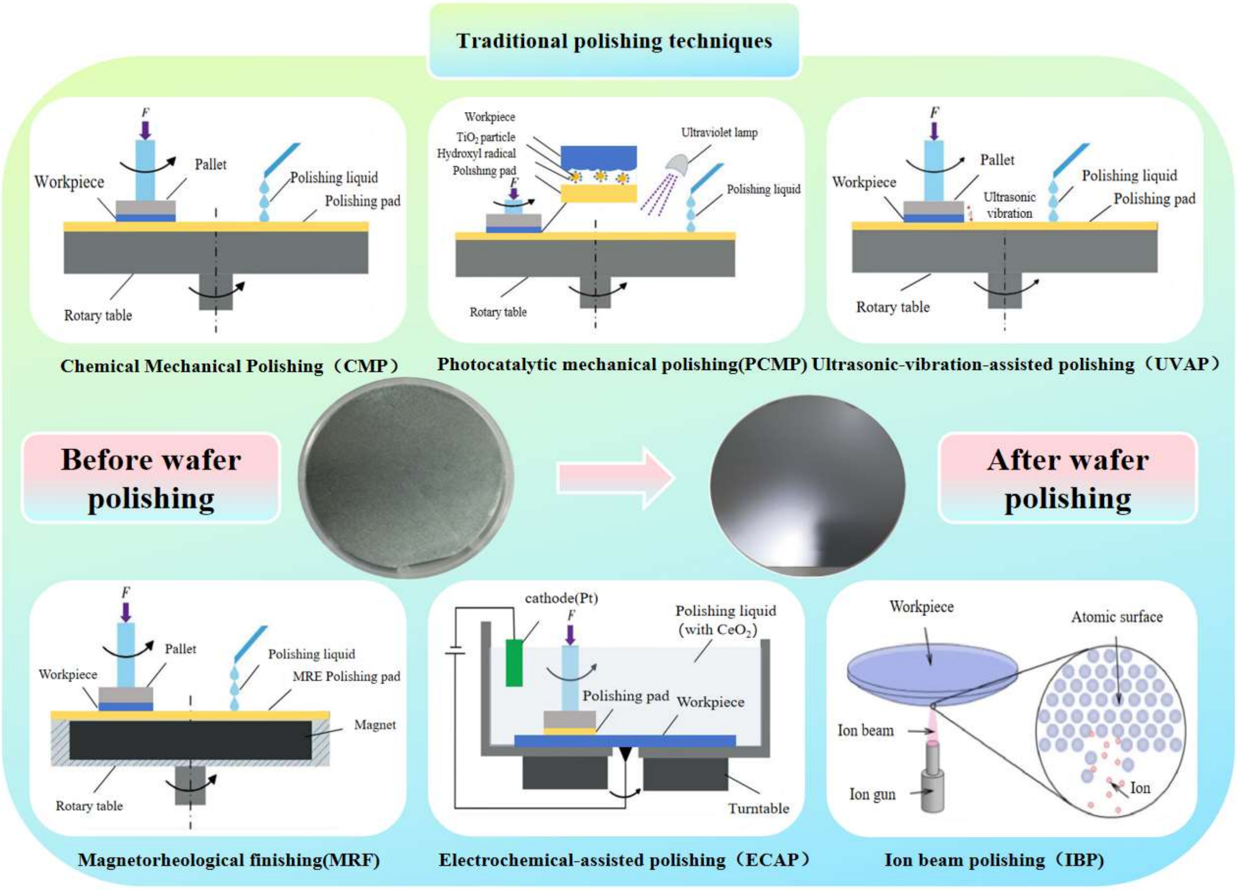

Figure 2. Conventional chip polishing technologies.

Although CMP technology has been widely used in semiconductor manufacturing and has achieved remarkable results, it still has some problems and limitations [30]. The CMP process requires complex polishing slurries and polishing pads, and the preparation of polishing slurries and the waste liquid treatment are expensive. In addition, although CMP has good uniformity on large-area wafers, it is still difficult to control uniformity at the microscale, especially when processing high-aspect-ratio structures. With the continuous improvement of the complexity and functional density of integrated circuits, multilayer interconnected structures have become increasingly important. Although CMP can achieve a certain degree of material selectivity, the selective removal of different materials in multilayer interconnected structures remains a challenge. These problems have prompted researchers to explore and develop new auxiliary polishing technologies to achieve higher material removal rates, lower surface roughness and good processing uniformity in order to replace or supplement the CMP process. UVAP was invented in the 1970s and began to be used in the polishing of high-hardness materials (such as ceramics and semiconductor materials) in the 1990s to improve material removal efficiency and surface quality. UVAP can improve upon the problems of surface damage and uniformity control that exist in the CMP process by introducing ultrasonic vibration [31,32]. The high-frequency vibration generated by ultrasound can significantly improve the fluidity and chemical reaction rate of the polishing liquid on a wafer’s surface, promote the contact between the polishing particles and the workpiece’s surface, reduce the effect of mechanical force and reduce surface damage, thereby improving the polishing efficiency (MRR reaching 500–5000 nm/h) and ensuring good surface quality (R_a of 1–5 nm). ECAP was born in the early 20th century, and it was applied in metal processing in the mid-20th century and gradually applied to the precision polishing of semiconductor materials in the late 20th century. ECAP technology uses electrochemical principles to produce anodic dissolution during the polishing process and combines mechanical friction to remove material and achieve surface polishing [33,34]. In the electrochemical process, the workpiece acts as an anode and undergoes an oxidation reaction in the electrolyte, dissolving the atoms on the surface of the material, which can achieve the selective removal of the material. The mechanical action helps to remove the reaction products and uneven parts on the surface, thereby obtaining a smooth surface (R_a of 1–10 nm). MRF was invented in the 1980s and began to be used for the precision polishing of optical lenses and semiconductor wafers in the mid-1990s. It was rapidly applied and promoted due to its high-precision processing effect. MRF uses a magnetic field to control the rheological properties of the polishing liquid to achieve high-precision surface polishing (R_a of 0.1–2 nm) [35–37]. MRF can control the amount of material removed at the nanometer level and is suitable for high-precision polishing of complex surfaces [38], but its polishing rate is slow (MRR of only 100–500 nm/h). PCMP was born in the early 2000s and has been gradually applied to the processing of high-precision optical surfaces and certain semiconductor materials in recent years. When a photocatalyst used in PCMP is exposed to light, electron-hole pairs are generated. These carriers migrate to the catalyst’s surface and react with water molecules or organic matter to generate highly oxidizing free radicals. These free radicals accelerate the chemical reactions on a material's surface, thereby improving polishing efficiency (MRR reaching 500–2000 nm/h) [39,40]. In addition, photocatalytic reactions can also reduce the use of chemical reagents and reduce environmental pollution. IBP was invented in the 1960s and began to be used in the semiconductor and high-precision optical fields in the late 1980s. It is suitable for processes with extremely high flatness requirements. As a direct processing method, IBP can achieve highly selective and high-precision surface polishing (R_a reaching 0.1–1 nm) by regulating an ion beam to precisely control the amount of material removed. It is suitable for processing high-aspect-ratio structures and complex surfaces, but its material removal rate is low (MRR of only 50–500 nm/h) [41]. The performance indicators of different polishing processes are shown in **Table 1**.

Table 1. Performance indicators of different chip polishing processes.

Type of process	Influencing factors	Material removal rate (MRR, nm/h)	Average roughness (R_a, nm)	Treatment uniformity	Merits	Shortcomings	References
Mechanical polishing (MP)	Mechanical force, abrasive particles	0.698–1.3	0.291–2	±10%–20%	Process is simple and cost is low	Surface damage is large and material selectivity is poor	[24,42]
Chemical mechanical polishing (CMP)	Mechanical force, chemical reactions, slurry composition	0.104–1.3	0.067–0.452	±2%–5%	High efficiency, good surface quality and good uniformity	Process is complex, cost is high, and waste liquid disposal is difficult	[26,27,31,43–46]
Ultrasonic-vibration-assisted polishing (UVAP)	Ultrasonic frequency and amplitude, polishing slurry	0.96–3.57	0.083–1.448	±5%–10%	High removal rate with low surface damage	Process is complex and equipment cost is high	[31,47]
Electrochemically assisted polishing (ECAP)	Voltage, current density, slurry composition	3–10	0.1–0.5	±5%–15%	Material selectivity is good, and surface damage is small	Process is complex and requires precise control of electrochemical parameters	[33,34]
Magnetorheological finishing (MRF)	Magnetic field strength, magnetorheological properties of polishing slurry	5.6–5.88	0.3–0.84	±1%–3%	High precision, suitable for complex surfaces	Process is complex and cost of magnetorheological fluid is high	[35,48]
Photocatalytic mechanical polishing (PCMP)	Light intensity, catalyst type, polishing slurry	0.238–0.95	0.054–0.489	±5%–10%	Environmentally friendly, reduce use of chemical reagents	Light sources and catalysts are required and process is complex	[39,49,50]
Ion beam polishing (IBP)	Ion beam energy and dose, angle	-	0.1–0.804	±1%–3%	High selectivity, high precision, suitable for high-aspect-ratio structures	Equipment cost is high, process is complex, and processing time is long	[41,51,52]

2.2. Plasma chip-polishing technologies

Although traditional chip polishing technologies can remove the raised parts of a surface and make the surface reach the required flatness and smoothness, these traditional polishing methods still have some limitations. Due to the high strength, high hardness and chemical stability of the substrate, most treatment methods that rely on surface oxidation have weak chemical reaction effects on the substrate, and the rate of generating a softened layer is low, resulting in a low MRR. In addition, the use of chemical reagents, such as polishing liquid and abrasives, also causes environmental problems. Therefore, efficient and green low-temperature plasma polishing has attracted much attention. This emerging technique uses the highly active particles of low-temperature plasma to finely process a chip's surface, which is expected to overcome many defects of traditional polishing processes and solve the problem of inconsistency between processing quality and polishing efficiency.

In view of the different characteristics of various low-temperature plasma chip polishing technologies, the different application levels of plasma are reviewed in this section and related technologies, which were plasma-assisted polishing (PAP), plasma electrolytic processing–mechanical polishing (PEP-MP), plasma chemical vaporization machining (PCVM) and plasma assisted selective etching (PASE), are elaborated. Among them, PAP and PEP-MP belong to auxiliary polishing technologies, which directly modify a substrate's surface through plasma or generate a softening layer through plasma electrolysis reaction, and then complete the treatment through mechanical polishing; PCVM and PASE belong to direct polishing technologies, which use the etching effect of plasma to directly complete the substrate treatment without the need for subsequent mechanical polishing process. The classification and principle of low-temperature plasma polishing technologies are shown in **Figure 3**.

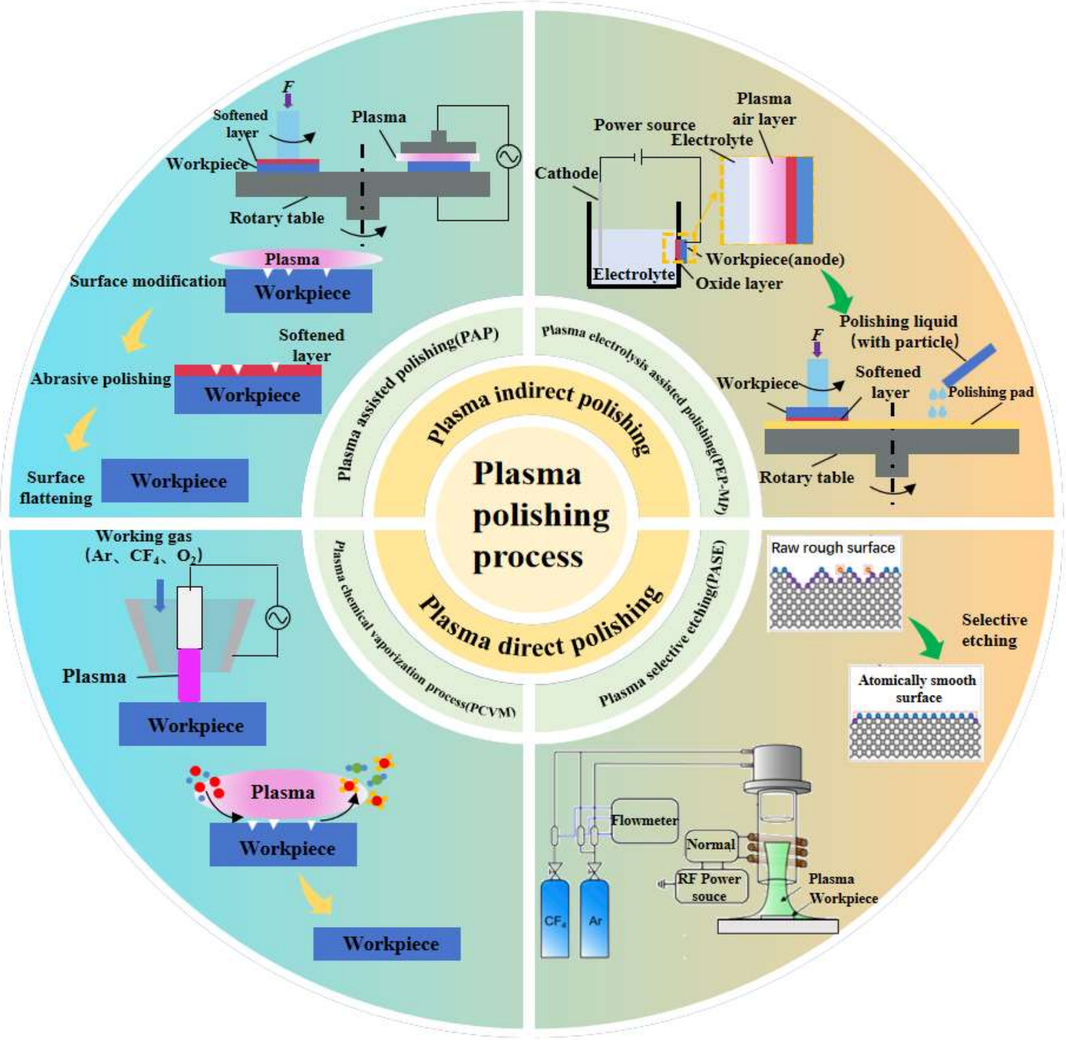

Figure 3. Classification and principles of plasma polishing technologies.

In addition, there are other plasma polishing technologies in the field of chip polishing, such as plasma-assisted cluster magnetorheological polishing (PACMP) and reactive atomic plasma processing (RAMP). PACMP technology combines plasma-assisted and magnetorheological polishing to achieve the micro-machining of a material's surface under precise control. This technology helps to improve processing accuracy and reduce surface defects in the chip manufacturing process, especially for micro-nanostructure surfaces with complex shapes. RAMP technology introduces highly reactive atomic plasma for the chemical removal of materials. It is suitable for scenarios that require high selectivity and low damage in chip manufacturing and can more effectively achieve material removal and fine patterning. This article focuses on the four technologies of PAP, PEP-MP, PCVM and PASE, mainly based on their wide application in chip manufacturing and the depth of research in existing literature. These four technologies have excellent performance in material removal rate, surface finish, processing efficiency, etc., and they are representative. They also have high technical maturity, covering different application scenarios, and can reflect the current development status and mainstream trends of low-temperature plasma polishing technology.

2.2.1. Plasma-assisted polishing (PAP)

PAP was first proposed by Yamamura et al. [53] in 2010. This technology combines plasma surface modification with mechanical polishing. It uses high-energy and high-activity particles generated by plasma to modify a substrate's surface, combined with the mechanical polishing process to achieve a high-efficiency and low-damage polishing effect.

(1) Principle of PAP technology

Chip materials can mainly include the following: silicon (Si), silicon carbide (SiC), gallium nitride (GaN), aluminum nitride (AlN) and single-crystal diamond (SCD). These materials have different application scenarios and requirements in chip manufacturing. Therefore, the principles of the PAP process used for different materials are also different, as shown in **Table 2**.

Table 2. PAP process for different substrate materials.

Base material	Surface hardness (HV)	Plasma working gases	Processing principle	References
Silicon (Si)	~1150	Hydrogen or fluorine-based gases	Silicon hydride or silicon fluoride is formed on substrate's surface	[54]
Silicon carbide (SiC)	~2500	Hydrogen-containing or oxygen-containing gases	Carbides or oxides are produced on surface of substrate	[54–57]
Gallium nitride (GaN)	~1400	Chlorine or fluorine gases	GaN or GaN is formed on substrate's surface	[58]
Aluminum nitride (AlN)	~2100	Fluorine gases	Aluminum fluoride is generated on substrate's surface	[57]
Single-crystal diamond (SCD)	~10,000	Oxygen-based gases	Oxidation of surface of polished plate	[25,59–61]

For materials with high hardness, such as Si, SiC, GaN, and AlN, plasmas that are oxygen-based, fluorine-based or chlorine-based are usually used to modify the materials' surface. During the modification process, a chemical reaction occurs on the surface of the substrate to form a softened layer. The hardness of the newly formed softened layer is much lower than the surface hardness of the original substrate. The substrate's surface is subsequently mechanically polished using soft abrasives. Since SCD has extremely high hardness and chemical stability, its polishing process is very challenging. Based on this, the PAP process of SCD takes a different approach. The removal mechanism of SCD in PAP is via the plasma-induced oxidation of the polishing plate's surface, the chemical reaction of the contact interface, and the wear of the contact interface. The plasma generates ·O or ·OH free radicals, and the polishing disc is treated to form a modified polishing interface on its surface. When the modified polishing disc interacts with the rotating diamond's surface, a chemical reaction occurs to form a composite chemical bond, and C atoms are removed under shearing action, thereby achieving the purpose of polishing.

- Higher-hardness substrates

When polishing higher-hardness substrates (such as Si, SiC, GaN and AlN), plasma is usually used to modify the surface to form a softening layer. The core of this process is that high-energy particles of plasma can undergo a series of physical and chemical reactions with the surface of the material. The softened layer formed is more easily removed by subsequent mechanical polishing. The chemical modification of the plasma and the friction removal of the polishing plate are carried out simultaneously, thereby obtaining a smooth surface at the atomic level without damaging the substrate's surface. For different substrate materials, different types of gases are doped in the plasma working gas to control the reactions occurring on the surface and the types of softening layer products ultimately generated.

For example, Deng and Yamamura [54], Deng et al. [55], and Ji et al. [56] used SiC as the substrate and irradiated its surface with atmospheric-pressure helium plasma containing water vapor or oxygen, as shown in **Figure 4a**. The free radicals in the plasma reacted with the SiC substrate's surface atoms, oxidizing the surface into a softened layer of about 80 nm thick composed of silicon dioxide (SiO_2) and Si-C-O bonds and reducing hardness from 37.4 ± 0.5 GPa to 4.5 ± 0.8 GPa. Ceric oxide (CeO_2) was then used as an abrasive to remove the modified layer by mechanical polishing, resulting in an MRR of about 80 nm/h, as shown in **Figure 4b**. Finally, an atomically smooth surface with a step structure was obtained, and surface roughness reached the subnanometer level without introducing scratches or crystallographic subsurface damage by using soft cerium abrasives (**Figure 4c**). Sun et al. [57] used AlN as a substrate and treated the surface with low-pressure argon mixed with carbon tetrafluoride plasma. The experimental setup is shown in **Figure 4d**. After 2 h of treatment, the substrate's surface was fluorinated and modified into aluminum fluoride, greatly reducing surface hardness. The surface was then polished using ceramic-bonded diamond as an abrasive, as shown in **Figure 4e**. During the polishing process, aluminum fluoride was removed, and a smooth AlN substrate's surface with surface roughness S_a of 3 nm and an MRR of 500 nm/h was obtained. Deng et al. [58] irradiated a GaN substrate's surface with atmospheric CF_4 plasma for 30 min and fluorinated the surface into a soft modified layer of GaF_3, significantly reducing surface hardness from 22.7 GPa to 13.9 GPa. Subsequently, CeO_2 was used as a mechanical polishing abrasive to mechanically polish the fluorinated and modified GaN substrate's surface. The overall process is shown in **Figure 4f**. No scratches were introduced after the plasma-assisted polishing of the GaN substrate's surface, and a very uniform stepped structure was obtained (S_z: 0.67 nm, S_q: 0.08 nm).

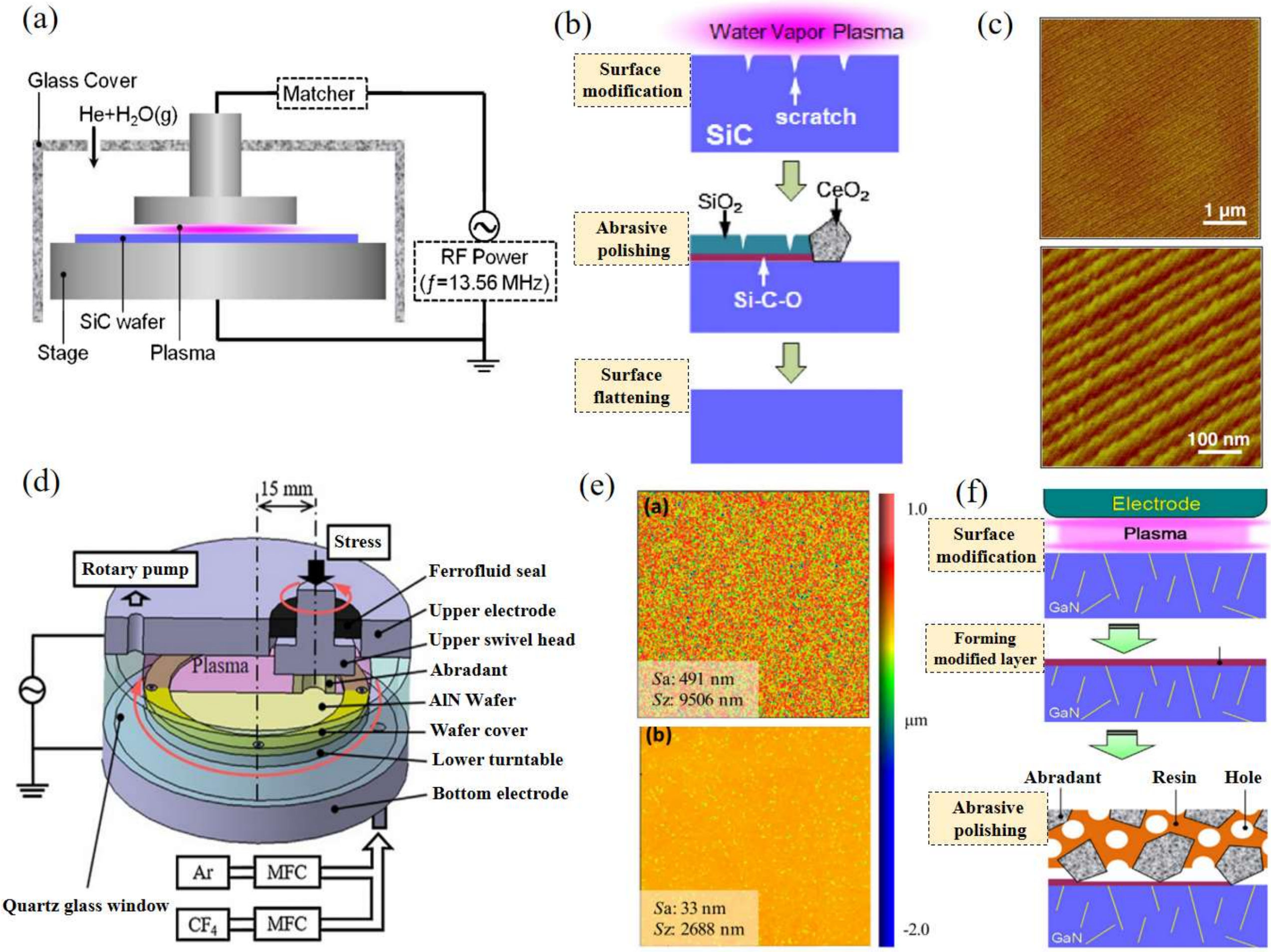

Figure 4. (a) Plasma treatment of SiC substrate [54]; **(b)** PAP treatment mechanism of SiC substrate [54]; **(c)** SiC substrate's surface before and after PAP treatment [55]; **(d)** PAP treatment of AlN wafer [57]; **(e)** AlN wafer's surface before and after PAP treatment [57]; **(f)** PAP treatment mechanism of GaN substrate [58].

- Very-high-hardness substrate (SCD)

An SCD substrate is usually treated indirectly by modifying the polishing plate with oxygen-based plasma. Therefore, the polishing plate's material has an important influence on the polishing effect. Peguiron et al. [59] found that when quartz glass was used as a polishing plate, and silicon dioxide and single-crystal diamond were ground together, Si-C bonds and O-C bonds with higher strength than C-C bonds were generated at the single-crystal diamond/silicon dioxide interface. Through the adsorption between Si-C bonds and the relative movement between the polishing plate and the single-crystal diamond, C atoms were removed, thereby polishing the single-crystal diamond. Based on this, Yamamura et al. [60] used argon plasma containing water vapor to treat quartz glass polishing plates. During the polishing process, the silicon atoms removed from the surface of the quartz glass were quickly oxidized and supplemented by O atoms generated by the plasma. Through plasma irradiation, the

MRR increased from 0.095 μm/h to 2.1 μm/h, which is 20 times that without plasma irradiation.

Luo et al. [61] developed an inductively coupled plasma (ICP) device to modify a silica polishing plate and also achieved SCD polishing, as shown in **Figure 5a**. The ICP produced a large number of ·OH radicals, which attached to the surface of the silica polishing plate. The modified polishing plate transferred -OH to the surface of the single-crystal diamond. The high-temperature plasma rapidly raised the temperature of the contact interface between the silicon wafer and the single-crystal diamond to several hundred degrees Celsius, providing sufficient activation energy for repairing chemical bonds. The -OH underwent dehydration and condensation reactions at the polishing interface to form chemical bonds, such as C-C, C-O, Si-O and C-O-Si, as shown in **Figure 5b**. Three main strong peaks of C1s, O1s and Si2p were detected via X-ray photoelectron spectroscopy (XPS) on the polished single-crystal diamond's surface. The chemical bonds corresponding to the areas of the three main strong peaks, as shown in **Figure 5c,** were consistent with the chemical bonds described in the material removal mechanism diagram in **Figure 5b**. Since silica is softer than single-crystal diamond, the silicon fragments that peeled off during the grinding process adhered to the surface of the single-crystal diamond. Therefore, Si-Si and Si-O bonds were also detected on the polished single-crystal diamond's surface. Generally, the C1s region determines changes in the surface chemical properties during the polishing process of single-crystal diamond. According to **Figure 5c**, the binding energy of the C-C bond was relatively weak. In addition, -OH easily adsorbed on the protrusions of the single-crystal diamond's matrix, and the bond energy at this position was relatively weak, so the protrusions can be easily removed by the chemical mechanical action. Therefore, the C atoms on the surface of the single-crystal diamond are removed under the shear friction between the two surfaces.

The subsequent mechanical polishing process in the PAP process also relies on the mechanical polishing process. Since MP may cause scratches or damage on the processed surface, Luo et al. [25] observed the surface morphology of SCD after polishing with quartz glass as the polishing plate, as shown in **Figure 5d**. After 3 h of plasma-assisted polishing, a very low surface roughness S_q was obtained, which was 0.14 nm, but many scratch-like structures were still observed on the SCD's surface. Therefore, a sapphire plate was selected as the polishing plate, and it was found that the surface was scratch-free after polishing, with S_q of 0.13 nm, as shown in **Figure 5e**. Hence, for SCD polishing, sapphire was found to be more suitable as a polishing plate than quartz glass. This was because the sapphire polishing disk became superhydrophilic under plasma irradiation, and Al-OH bonding groups were generated on the surface. Subsequently, C atoms on the SCD's surface reacted with hydroxyl groups on the polishing plate's surface to form C-O-Al. The chemical bonds generated by this reaction reacted with the quartz glass plate and the single-crystal diamond's surface to form C-O-Si bonds. Si-O bonds and O-C bonds were easier to remove, which was beneficial for the subsequent mechanical removal of carbon atoms on the single-crystal diamond's surface through the relative movement between the single-crystal diamond and the polishing plate, as shown in **Figure 5f**.

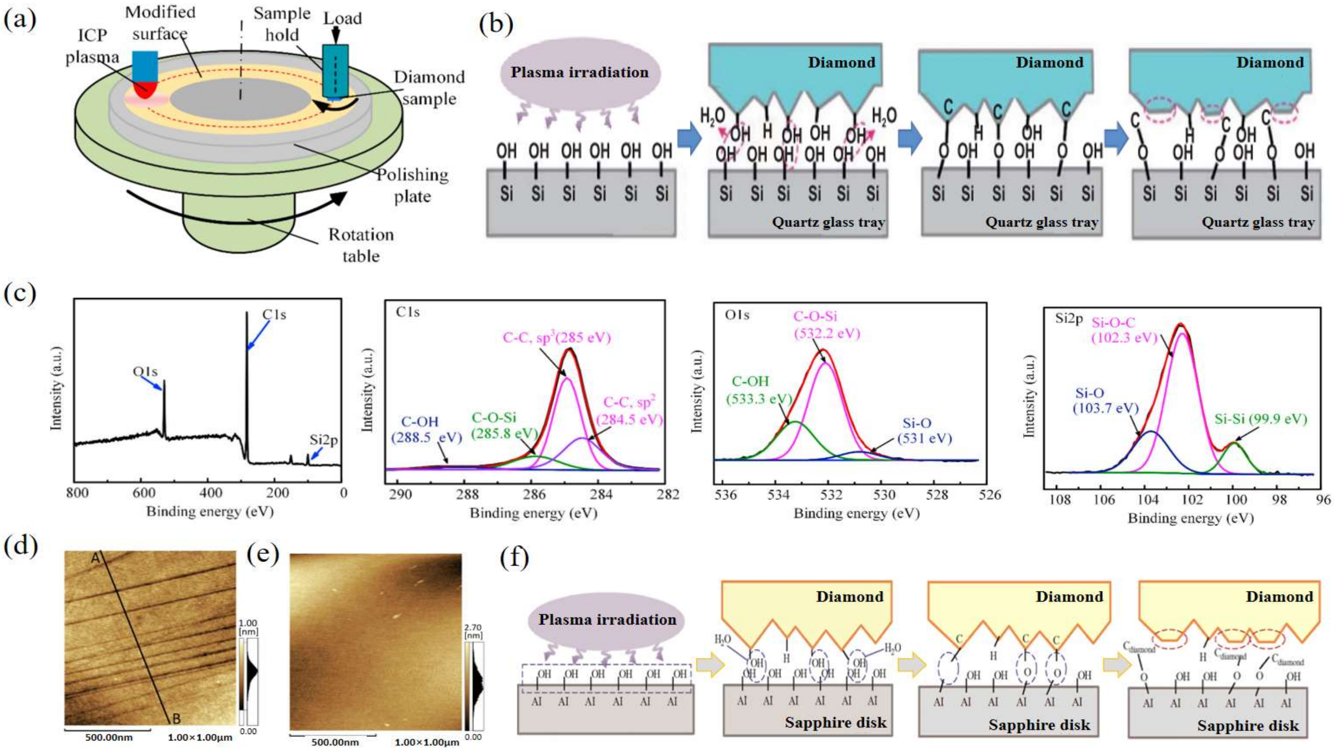

Figure 5. PAP treatment of SCD substrate: **(a)** ICP polishing of SCD [61]; **(b)** SCD removal mechanism when quartz glass was used as polishing plate [61]; **(c)** XPS fractionation of C1s, O1s and Si2p on SCD's surface when quartz glass was used as polishing plate [61]; **(d)** surface morphology of SCD polished with quartz glass as polishing plate [25]; **(e)** surface morphology of SCD polished with sapphire as polishing plate [25], and **(f)** removal mechanism of SCD when using sapphire as polishing plate [25].

(2) Effects of different process parameters on PAP

PAP technology achieves precise polishing by irradiating a workpiece's surface with plasma and then mechanically polishing it. However, the polishing effect of PAP is affected by a variety of process parameters, which are mainly divided into front-end plasma modification effect control and back-end mechanical polishing control.

In the plasma modification process, RF power is usually used to generate high uniformity, high density and high activity plasma. Generally speaking, the higher the density of active particles contained in the plasma, the resulting MRR will be higher. Therefore, increasing the density of active species in plasma is the focus of researchers. Ji et al. [56] found that, when using water vapor as the reactive gas, the MRR of a SiC substrate's surface was significantly higher than when using O_2 as the reactive gas. Comparing the plasma emission spectra of the two (**Figure 6a**), water vapor as the working gas generated ·OH radicals with high intensity (oxidation potential of 2.80 eV) after ionization, which was stronger than ·O radicals generated by O_2 ionization (oxidation potential of 2.42 eV), indicating a higher oxidation ability. So, the MRR when using water vapor as the reactive gas was higher than the MRR when using O_2 as the reactive gas.

Mechanical polishing, as the back-end link of plasma modification, directly determines the polishing effect and product quality. The process parameters that affect mechanical polishing are mainly mechanical polishing pressure and sliding speed. Mechanical polishing pressure determines the contact form between a polishing disk and a substrate, and sliding speed determines the contact frequency between the polishing disk and the substrate. Taking SCD as an example, Liu et al. [62] found that the surface roughness of the substrate after polishing was different under different mechanical polishing pressures. Under a low polishing pressure (62.5 kPa), the material removal followed the conventional mechanism, the isotropic removal effect was dominant, and the average surface roughness S_q after polishing was about 0.30 nm; under a high polishing pressure (350.0 kPa), the contact area between the SCD substrate and the polishing plate was converted into graphite due to the high temperature and high pressure. At the same time, the shear force generated by the relative rotation of the SCD substrate and the polishing plate separated the newly generated non-diamond layer from the surface, as shown in **Figure 6b**. In this process, the protruding area on the SCD substrate was preferentially graphitized and separated, resulting in a smooth surface. The average surface roughness S_q after polishing was about 0.55 nm. In addition, the polishing disk rotation speed had no significant effect on the surface quality of the SCD processed by PAP. The MRR increased with the increase in polishing pressure and rotation speed, as shown in **Figure 6c**. The maximum MRR reached 5.3 μm/h, which was achieved by increasing the scratching frequency between the polishing plate and the SCD substrate.

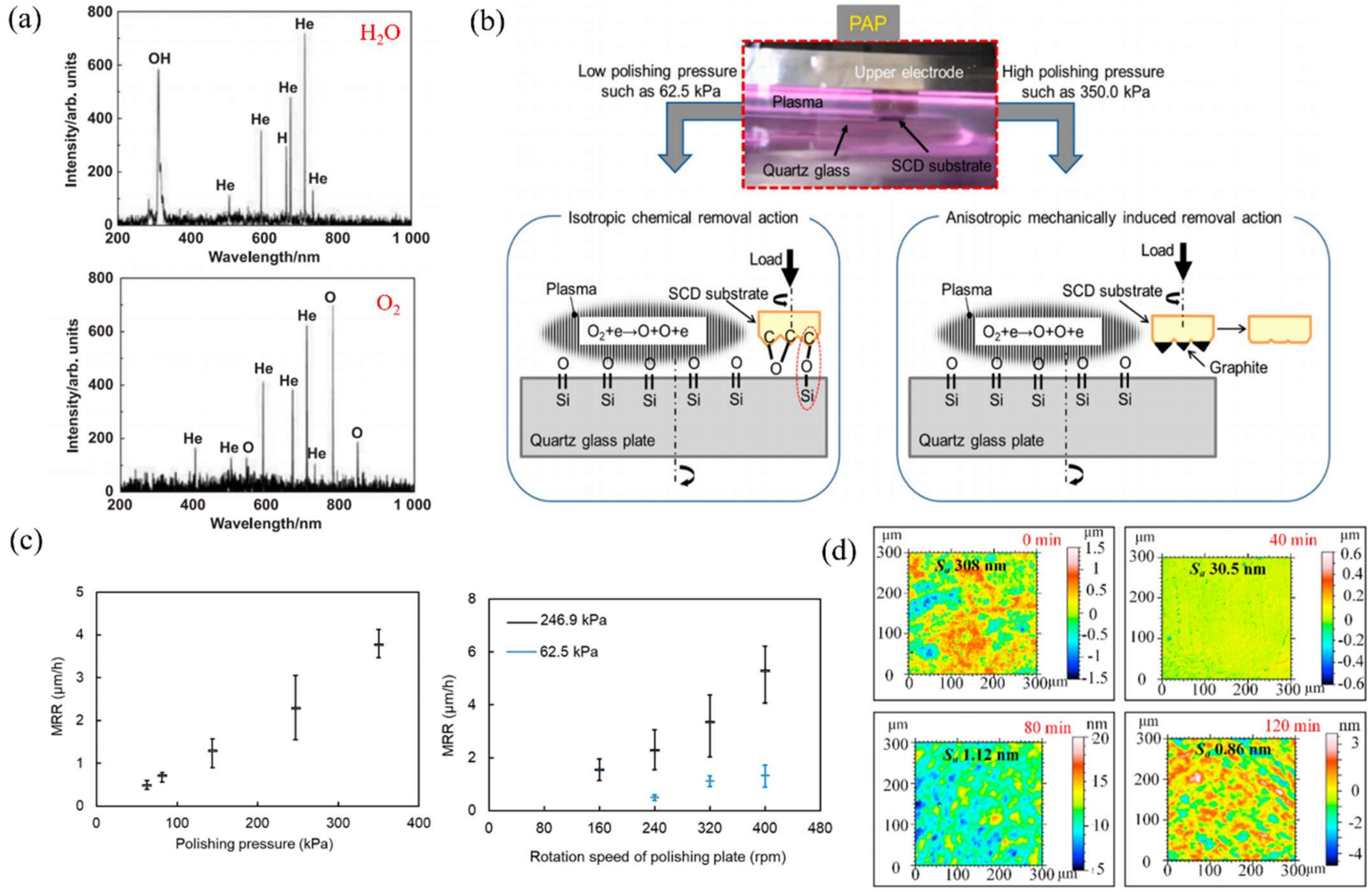

Figure 6. (a) Emission spectra of water vapor and oxygen as reaction gases [56]; **(b)** Quartz glass removal mechanism under different polishing mechanical pressures [62]; **(c)** Variation of MRR with polishing pressure and rotational speed [62]; **(d)** Surface quality with different polishing times [25].

In addition, plasma irradiation will introduce some small peaks and valleys, and the mechanical grinding action of a polishing disk will also leave scratches on a substrate's surface. Therefore, in the early stage of the polishing process, the substrate's surface is rough. When the polishing time is long enough, the polishing quality of PAP can meet usage requirements. Luo et al. [25] studied the change in the surface roughness of an SCD substrate with polishing time in PAP. Under 40 min, the surface roughness of the substrate was greater than 30 nm, as shown in **Figure 6d**. When the polishing time reached 120 min, surface roughness S_a of the SCD reached 0.86 nm. This shows that polishing time has a significant effect on the polishing quality in PAP. When the polishing time is sufficient, the surface accuracy of a substrate can meet the requirements.

(3) Summary

During the PAP process, chips of different materials all use high-energy and highly active particles of plasma to modify or soften the material's surface, so the PAP process is widely applicable. The specific process varies according to the chemical properties of the material and the type of plasma used, but the overall goal is to further remove surface defects and roughness through mechanical polishing after plasma treatment to obtain a surface with high flatness and finish.

Although CMP provides low-damage treatment, its resulting MRR is too low. In addition, the obvious anisotropy of the CMP material removal process leads to a weak flattening ability at the atomic scale. In contrast, in the PAP treatment of substrates except SCD, the use of a large amount of chemical reagents is avoided and the pollution to the environment is reduced; when the PAP treatment of SCD, the plasma in PAP only modifies the polishing plate, and material removal mainly depends on the chemical reaction and wear at the contact interface between the polishing plate and the diamond. Therefore, PAP combines the advantages of MP and CMP to achieve efficient and high-quality surface polishing.

Although PAP technology has shown many advantages in chip material processing, its large-scale application still faces some challenges, such as the stability of the plasma source, optimization of process parameters, equipment cost and integration of plasma processing and mechanical polishing. Future research will focus on improving the stability and efficiency of PAP technology and exploring new plasma sources and process parameters to achieve more efficient and precise polishing of a chip material's surface.

2.2.2. Plasma electrolytic processing-mechanical polishing (PEP-MP)

PEP is a special electrochemical polishing process under high-voltage and salt solution conditions. As an innovative polishing technology, PEP is widely used in the field of metal polishing. It can make a metal's surface smooth and shiny in a short time, making it more corrosion-resistant [63,64]. In 2021, Ma et al. [65] proposed a new PEP-MP technology that combines PEP with MP. This technology uses the PEP process to form a softened layer on a substrate's surface, which is then removed by MP to achieve the surface polishing of the chip material.

(1) Principle of PEP-MP technology

PEP-MP is divided into two processes, which are plasma electrolysis and mechanical polishing, as shown in **Figure 7a**. The surface of a chip material is modified into a relatively soft oxide layer by plasma electrolysis treatment and then mechanically removed using a soft abrasive. Since the hardness of a soft abrasive is lower than that of a substrate material's surface, only the softened layer will be removed during the mechanical polishing process, causing no scratches or damage to the substrate's surface.

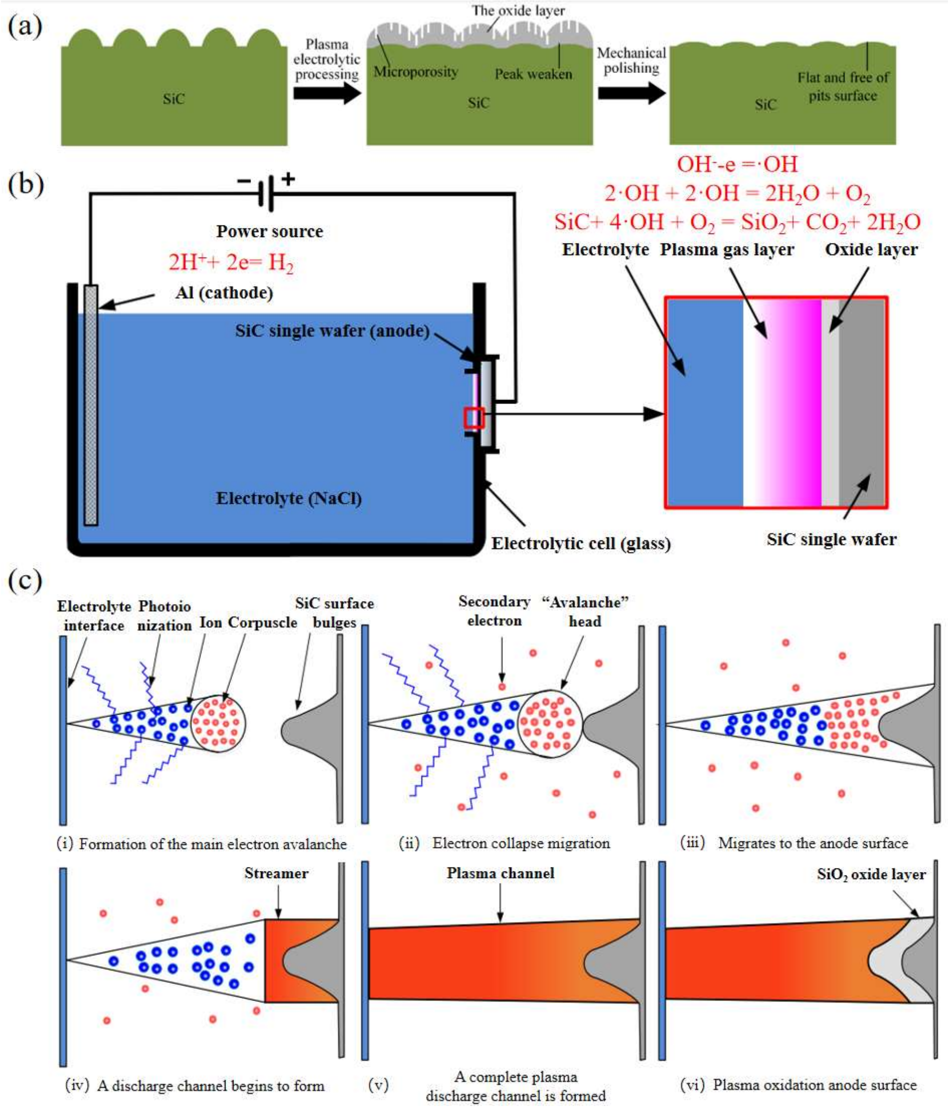

Figure 7. (a) Plasma electrolytic treatment and polishing process [65]; **(b)** Plasma electrolytic treatment device [65]; **(c)** Micro-schematic diagram of plasma oxidation process of SiC electrolytes [66].

Ma et al. [65] used PEP-MP for the plasma electrolysis treatment and mechanical polishing of the oxide layer of a microcrystalline 4H-SiC substrate's surface. First, the surface of the single-crystal 4H-SiC substrate was modified by PEP treatment into a soft oxide layer mainly composed of silicon dioxide. The device is shown in **Figure 7b**. The overall device consisted of a power supply, an electrolyte, a cathode, a single-crystal 4H-SiC anode, and an insulating glass electrolytic cell. When the system was charged with an appropriate current, the instantaneous short circuit of the system caused electrolytes at the position in contact with the workpiece to evaporate, generating a gas envelope composed of water vapor to wrap the part and isolate the part from the electrolyte [66]. Under the action of a high electric field, electrons at the interface of the electrolytes and the gas envelope were accelerated instantaneously, gaining enough speed and energy to rush to the surface of the part. Then, the electrons collided directly with water vapor molecules in the gas envelope to release other electrons. These electrons hit other water vapor molecules to form an electron avalanche. After that, the flow of electrons and ions formed a conductive channel connecting the surface of the part to the electrolyte. The channel is filled with high-temperature plasma, called a plasma gas layer, as shown in **Figure 7c**. This process also brought about complex physical and chemical effects, including the generation of ultraviolet rays, shock waves and ultrasonic cavitation. Active substances, such as hydroxyl radicals (·OH), oxygen radicals (·O), hydroperoxide radicals ($\cdot HO_2$), H_2O_2 and O_3, were produced by chemical reactions. Active substances ·OH, ·O and $\cdot HO_2$ bombarded the surface of the part through the discharge channel and reacted to form an oxide film. The active substance ·OH has a strong oxidizing property (oxidation potential of 2.8 eV), but it is very unstable. Some ·OH reacted to produce water and oxygen, and some ·OH reacted with the single-crystal 4H-SiC substrate to produce silicon dioxide.

Around the scratch and pit regions, a large number of covalent bonds formed between carbon atoms and adjacent silicon atoms were broken, resulting in a large number of dangling bonds, free electrons and holes. Therefore, the scratch and pit regions had a high density of available charge carriers, which greatly improved the conductivity of these regions, leading to preferential oxidation of these regions. At the same time, the plasma gas layer had different thicknesses at the protruding and recessed positions of the substrate, resulting in a higher current density at the protruding positions, which obtained a higher oxidation rate [67]. Therefore, the MRR from mechanical polishing after plasma electrolysis treatment was higher, leading to a rapid smoothing effect.

(2) Effects of different process parameters on PEP-MP

Due to the presence of a water vapor gas envelope near the anode, the discharge between the anode and the electrolyte is a gas discharge. Therefore, its discharge mode is crucial for the formation of the softening layer. Ma et al. [65] distinguished three main discharge types based on the current, as shown in **Figure 8a**: Townsend discharge (B-C), glow discharge (D-E) and arc discharge (G-H). In addition, there are four transition zones: non-self-sustaining discharge zone (A-B), subnormal glow discharge (C-D), abnormal glow discharge (E-F), and transition to arc (F-G). By adjusting different discharge modes and observing the final polishing effect, it was found that after the oxide layer was formed in the E-F region, an ultra-smooth surface was obtained but its MRR was low; while in the F-G region, a high MRR was obtained. There were more surface pits caused by arc discharge, indicating that the discharge modes corresponding to these two regions were not suitable for the surface softening of chip materials. In the abnormal glow discharge region (E-F), $dU/dI > 0$, while in the region of the transition to the arc (F-G), $dU/dI < 0$. Therefore, there must be a region near F where dU/dI approached 0. The gas ionization rate and plasma generation rate in this region were just suitable for semiconductor surface softening.

While ensuring surface quality, a high MRR can be obtained. This region is called the micro-arc plasma discharge region. By adjusting plasma discharge parameters to maintain the oxide layer's formation in the micro-arc plasma discharge region, the SiC substrate's surface was oxidized to SiO_2, and its surface hardness decreased from the initial 2891.03 HV to 72.61 HV. The thickness of the oxide layer was about 2 μm, as shown in **Figure 8b**. Comparing the three-dimensional morphology of samples before and after the PEP-MP treatment, it was found that there were many deep scratches, pits and peaks on the surface of the sample before treatment, and its surface roughness was poor (S_z of 607 nm and R_a of 64.5 nm); after polishing, the deep scratches, pits and peaks basically disappeared, and S_z was 60.1 nm and R_a was 8.1 nm, as shown in **Figure 8c**. The calculated MRR from PEP-MP was about 21.8 μm/h, indicating that PEP-MP is an efficient chip surface polishing technology.

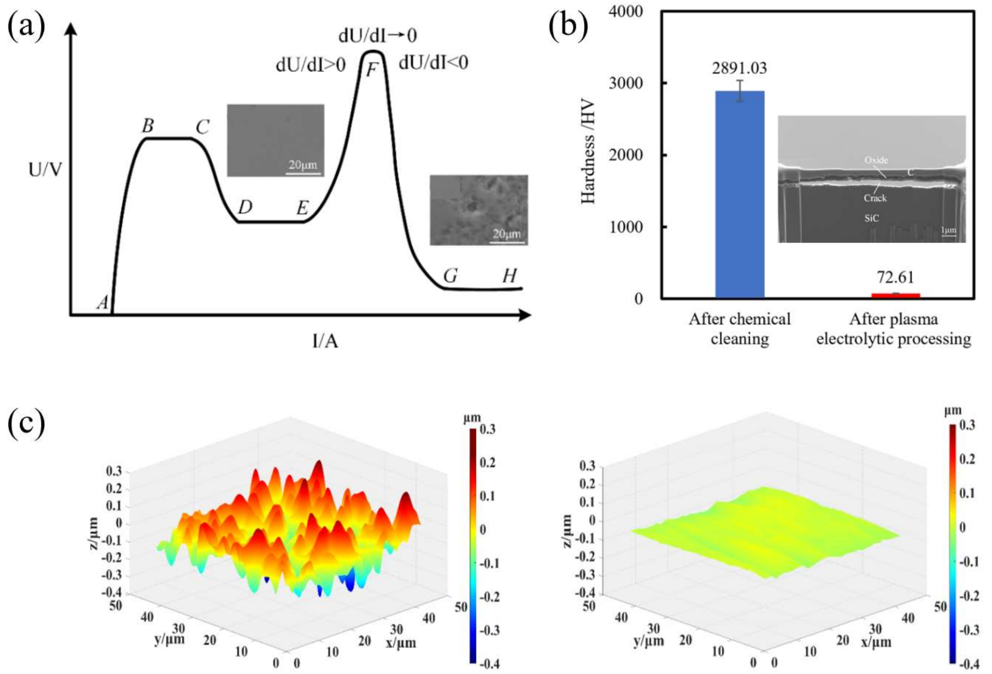

Figure 8. (a) Surface morphology under different discharge modes [65]; **(b)** Hardness of oxide layer formed by plasma electrolysis processing decreased dramatically [65]; **(c)** Three-dimensional morphology of samples before and after plasma electrolysis processing and mechanical polishing treatment [65].

(3) Summary

As an emerging polishing technology, PEP-MP exhibits an ultra-high MRR and significantly improves polishing efficiency. Different from the alternating cycle of plasma treatment and mechanical polishing in PAP technology, PEP-MP implements a process of plasma electrolytic treatment followed by mechanical polishing. However, the continuous growth of the softening layer may lead to poor surface quality. Hence, further research is required on the control mechanism of the growth of the interface softening layer. At present, in the field of chip materials, PEP-MP is only applied in SiC, and its application scope needs to be broadened in the future. In addition, studies have shown that ultrasonic vibration can promote the plasma oxidation effect on a workpiece's surface and has been used in the field of plasma electrolytic polishing of metal parts [68]. This technology can also be integrated into PEP-MP to further improve polishing efficiency.

2.2.3. Plasma chemical vaporization machining (PCVM)

Unlike PAP and PEP-MP, which use plasma to modify a substrate's surface to form a softening layer, PCVM uses active species generated in the plasma to directly react with the substrate to generate gaseous products, which is a gas-phase chemical etching method. Since the subsequent mechanical polishing process is omitted, PCVM has a higher polishing efficiency and is suitable for efficient and fast processing.

(1) Principle of PCVM technology

PCVM is a direct polishing technology that uses the high-energy characteristics of plasma to etch a material's surface, thereby achieving high-precision material removal and surface modification [69]. This technology uses the high-energy active particles generated by plasma to trigger a series of chemical reactions on the material's surface, converting the solid material into volatile gaseous products, thereby removing the surface layer of the material. In these reactions, the high-temperature characteristics of the plasma can not only dissociate the gas to generate highly active atoms (such as fluorine, chlorine, oxygen and hydrogen) but also reduce the activation energy of the reaction and enhance the material removal rate. The high-temperature environment also promotes the exothermic reaction, allowing products (such as SiF_4, $SiCl_4$, CO_2 and CO) to escape quickly, thereby improving the surface cleaning effect and processing efficiency. This high-temperature characteristic combined with the exothermic reaction mechanism enables the plasma polishing technology to remove materials efficiently and with low damage at the nanometer level. Like PAP, PCVM has a strong selectivity for reactive gases. For different substrate materials, appropriate reactive gases need to be selected, as shown in **Table 3**.

Table 3. PCVM process for different substrate materials.

Base material	Reactive gases	Basal surface reactions	Reaction enthalpy (kJ/mol)	Reference
Silicon (Si)	Fluorine gases (e.g., SF_6, CF_4)	$Si+4F \rightarrow SiF_4$	–1615	[69]
Silicon carbide (SiC)	Chlorine gases (e.g., Cl_2)	$SiC+2Cl_2 \rightarrow SiCl_4+C$ $C+O \rightarrow CO$ $C+2O \rightarrow CO_2$	–657 –110 –394	[70]
	Fluorine gas (e.g., SF_6, CF_4)	$Si+4F \rightarrow SiF_4$ $C+O \rightarrow CO$ $C+2O \rightarrow CO_2$	–1615 –110 –394	[71]
Gallium nitride (GaN)	Chlorine gases (e.g., Cl_2, BCl_3)	$2GaN+3Cl_2 \rightarrow 2GaCl_3+N_2$ $2GaN+3BCl_3 \rightarrow 2GaCl_3+3BN$	–950 –530	[70]
Diamond (SCD)	Oxygen (O_2) or hydrogen (H_2)	$C+O \rightarrow CO$ $C+2O \rightarrow CO_2$ $C+4H \rightarrow CH_4$	–110 –394 –74.8	[72]

Yamamura et al. [71] introduced an inert gas (He) and a reactive gas ($CF_4 + O_2$) into a reaction system, which generated plasma through high-frequency electric field excitation to polish and remove a SiC substrate's surface using active free radicals generated in the atmospheric-pressure plasma, as shown in **Figure 9a**. The inert gas provided the necessary active environment for exciting the reactive gas, and the excited reactive gas produced particles with extremely high chemical activity. These highly active particles reacted chemically with atoms on the surface of the SiC substrate to generate volatile compounds, such as silicon tetrafluoride (SiF_4) and carbon dioxide (CO_2). In addition, the reaction was a highly exothermic reaction, and the generated gaseous products were stable. In addition, the high temperature in the plasma helped to decompose fluorine compounds (such as CF_4) and generate highly active fluorine atoms, which reacted quickly with silicon, thereby improving removal efficiency. While the gaseous compounds were generated, these gases were continuously released, thereby achieving effective material removal, with an MRR of up to 1.8 μm/min.

For a GaN substrate, chlorine-based gases are usually used as working gases instead of fluorine-based gases. Because the boiling point of the reaction product GaF_3 when using fluorine-based gas is about 1000 °C, the reaction product will not evaporate but remain on the substrate's surface, inhibiting the etching reaction and deteriorating the surface flatness after etching; when using Cl_2, the boiling point of $GaCl_3$ is about 201 °C. By heating the substrate above its boiling point, the reaction product easily evaporates from the substrate's surface. Moreover, this reaction is an exothermic reaction. The high temperature of the plasma makes the chlorination reaction of the GaN substrate's surface more rapid, and nitrogen is generated as a by-product. Since chlorine atoms are extremely active at high temperatures, this chemical reaction is significantly accelerated under plasma-assisted conditions, thereby effectively removing the surface of the GaN substrate. Therefore, Cl_2 has been selected as the reaction gas for etching GaN substrates, and inert gas (such as He) has been used to generate and maintain a stable plasma at atmospheric pressure. Nakahama et al. [70] successfully achieved the etching of a GaN substrate's surface by mixing He with Cl_2. As shown in **Figure 9b**, the MRR reached up to 9.1 μm/min, but the diameter of the processed area was only 4–5 mm.

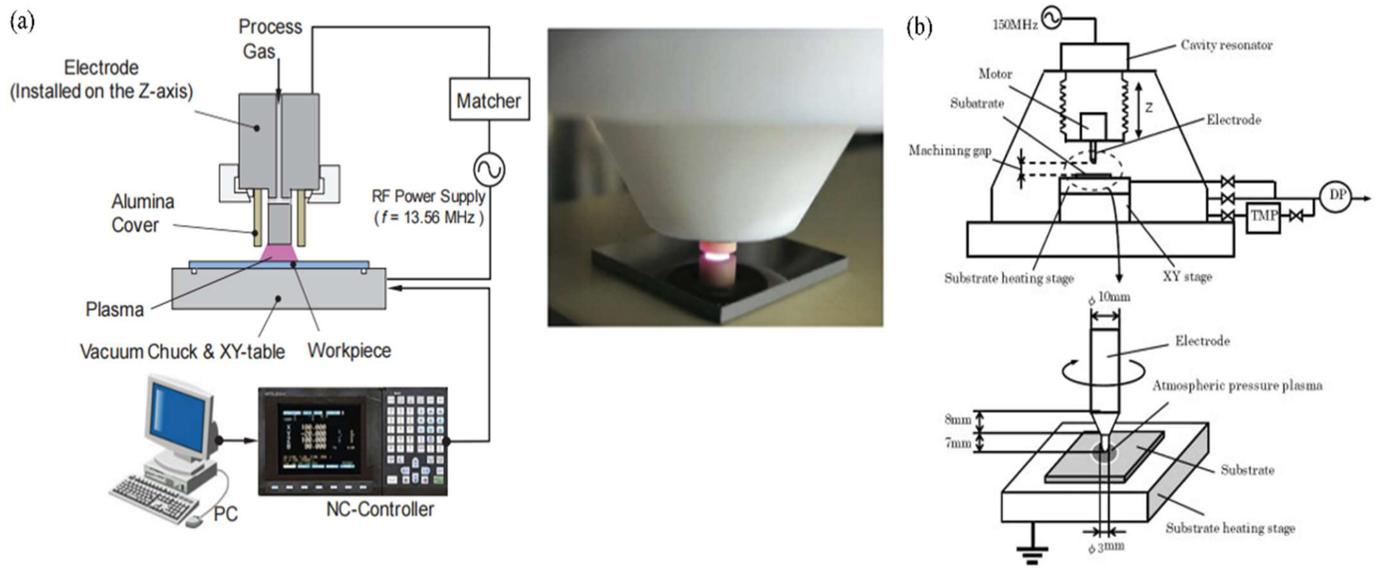

Figure 9. (a) PCVM treatment of SiC substrate [71]; **(b)** PCVM treatment of GaN substrate [70].

(2) Effects of different process parameters on PCVM

PCVM uses active species generated in plasma to directly react with a substrate to generate gaseous products. Therefore, increasing the content of active species in plasma to obtain a larger MRR has become the focus of researchers.

On the one hand, the content of active species in plasma can be increased by increasing the partial pressure of the reactive gas in the plasma. Yamamura et al. [71] found that the MRR of a SiC material increased with the increase in the $O_2/(O_2 + CF_4)$ ratio, as shown in **Figure 10a**. When the ratio of O_2 and CF_4 was uniform, the MRR reached a maximum value of 1.8 μm/min. This was because SiC is not easily etched under the action of pure fluorine free radicals. After the introduction of oxygen, the SiC substrate's surface first underwent an oxidation reaction to generate SiO_2 and CO_2. The generated SiO_2 reacted with fluorine free radicals to further generate SiF_4 and O_2, thereby promoting the removal of material. Nakahama et al. [70] found that the removal depth of a GaN material increased with the increase in Cl_2 partial pressure, as shown in **Figure 10b**. When the Cl_2 concentration was 2%, the removal depth was much greater than that at other concentrations. Therefore, a flow field disturbance was formed by rotating the high-voltage electrode to effectively provide a large amount of Cl_2 to the plasma area so that the reaction gas in the plasma area was effectively replenished.

On the other hand, the plasma ionization degree and energy density can be increased by increasing the power of the plasma excitation power supply. By increasing RF voltage, the electric field strength in the plasma is enhanced, thereby increasing the kinetic energy of the charged particles. The increase in the average energy of the plasma can enhance ion bombardment intensity and the density of active particles, which can effectively activate the substrate's surface, thereby improving the chemical reaction activity of the material and ultimately accelerating the increase in the MRR under high-power conditions. Sano et al. [69] compared the effects of different RF powers on the MRR of Si and SiC substrates and found that the MRRs of both increased with increasing RF power, as shown in **Figure 10c**. The MRR of the Si substrate increased almost linearly, while the MRR of the SiC substrate increased at a higher rate at a higher RF power. This was because the SiC substrate had a higher chemical stability and a more complex crystal structure than those of the Si substrate, so its reactivity to plasma was lower than that of silicon. At a lower RF power, more energy was required to break SiC's chemical bonds. As the RF power increased, more energy was used to activate the chemical bonds, resulting in an increase in the MRR at a higher power.

In addition, when the etching rate is increased by increasing the plasma power, the thermal stress caused by the local temperature increase may cause a substrate to crack. Nakanishi et al. [72] found that when the temperature of a local area of a wafer increased due to the increase in power, the depth and width of the etch pit also increased, and the uneven substrate temperature led to a decrease in polishing quality, as shown in **Figure 10d**. Therefore, in the PCVM process, uniform heating of a substrate is an effective technology to improve its MRR and polishing quality. Ueda et al. [73] found that with the increase in the surface temperature of a quartz wafer, the $He/CF_4/O_2$ plasma etching rate increases exponentially, and the removal depth at 80 °C was 1.5 times that at 40 °C, as shown in **Figure 10e**. Through the activation of the plasma, He/CF_4/O_2 dissociated into highly active fluorine atoms and oxygen atoms, which reacted chemically with the wafer's surface to generate volatile products. Among them, fluorine atoms reacted with silicon atoms on the quartz's surface to generate SiF_4, and oxygen atoms combined with carbon that may remain on the surface to generate CO_2. The volatility of these products proved that the removal process of quartz crystals in the PCVM process was chemically reactive. This reactivity ensured the efficient removal of materials and verified the reactive nature of the PCVM process. Furthermore, the change in the etching rate as a function of temperature follows the Arrhenius law, as shown in **Figure 10f**. When combining the properties of the reactants with the characteristics of the reaction products, the chemical reactivity in the removal process was further verified, which shows that the removal reaction of quartz crystals by PCVM is a chemical reaction.

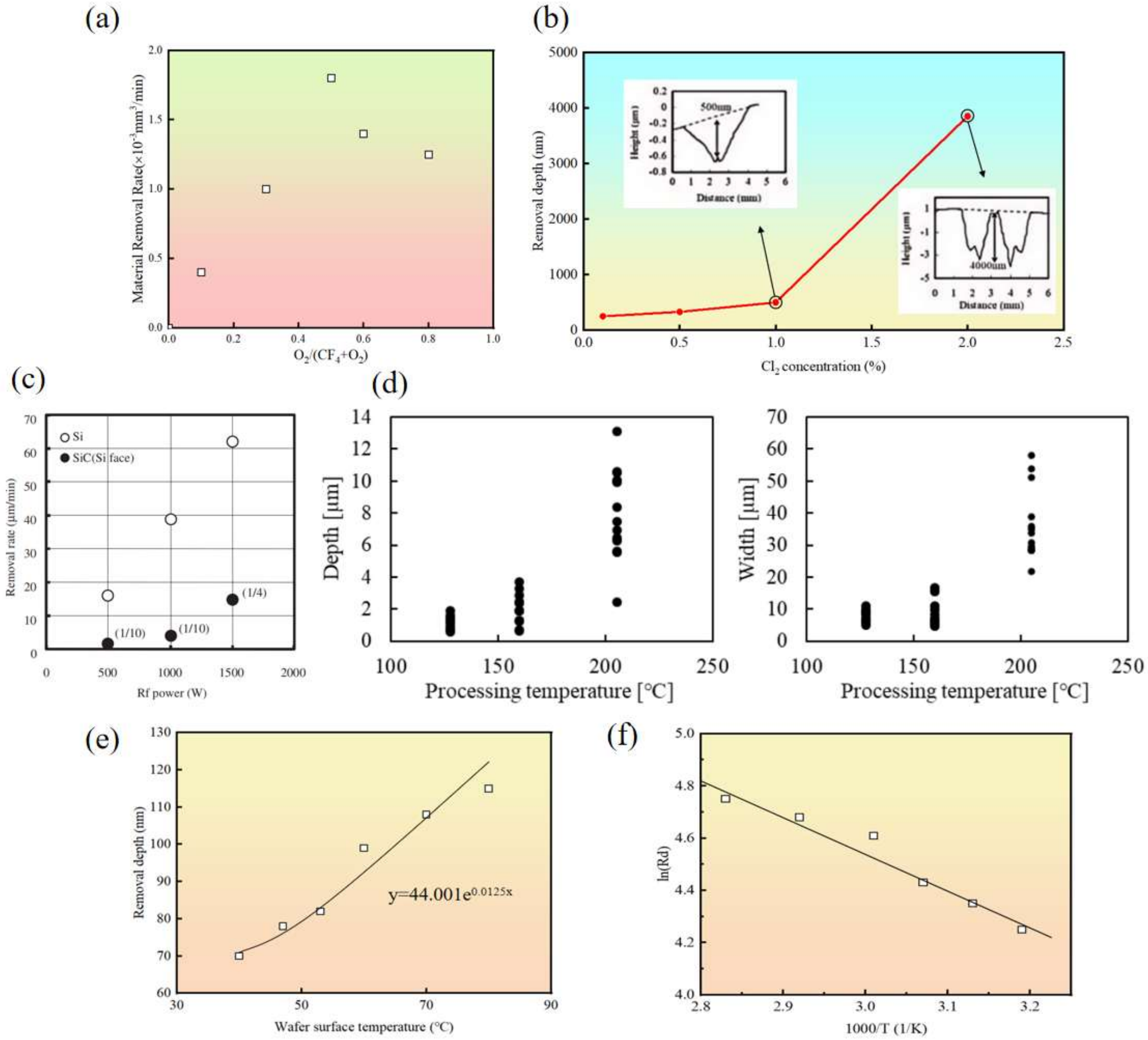

Figure 10. (a) SiC substrate's MRR with $O_2/(O_2 + CF_4)$ change [71]; **(b)** GaN substrate's removal depth with Cl_2 content change [70]; **(c)** Si and SiC substrates' MRR with RF power change [69]; **(d)** Removal depth and width with substrate temperature change [72]; **(e)** Quartz wafer's removal depth with substrate temperature change [73]; **(f)** Removal rate with substrate temperature change [73].

(3) Summary

Since no mechanical contact is required, PCVM avoids stress and deformation that may be introduced in mechanical polishing. Moreover, PCVM only relies on the chemical reaction on a substrate's surface and has no physical etching effect. Therefore, it is suitable for precision machining with extremely high surface requirements. Compared with chemical mechanical polishing, PCVM reduces the dependence on chemical reagents and reduces the risk of environmental pollution.

Comparing the MRRs from different processes, it has been found that the MRR from PCVM is much higher than those from PAP and PEP-MP. However, it is necessary to compare the processing time of a substrate of the same size to evaluate the practicality of PCVM. For PAP and PEP-MP, large-area substrates can be processed at the same time, while PCVM is limited by the size of the plasma electrode and can only complete the processing within a limited area. Although its MRR is high, it takes longer to process large-area substrates. Therefore, the development direction of PCVM is to expand the electrode's size and optimize the electrode's shape to generate large-area uniform plasma to process large-area substrates to shorten the processing time. In addition, accurately controlling the energy distribution and range of action of plasma and adjusting the process parameters when processing different materials to pursue better surface quality are also challenges faced by large-scale applications of PCVM.

2.2.4. Plasma assisted selective etching (PASE)

With the rapid development of the semiconductor industry, especially integrated circuit manufacturing technology, although PCVM technology can achieve efficient material removal, the challenges faced by PCVM increase when the etching rate and etching depth need to be precisely controlled and surface roughness requirements are high. In response to this situation, Fang et al. [74] proposed PASE technology in 2020 as a new polishing method for chip materials.

(1) Principles of PASE technology

The PASE process uses atmospheric-pressure inductively coupled plasma (ICP) for processing because it provides an environment of high-temperature and high-density free radicals, which is crucial for accelerating the chemical reaction of atoms on a substrate's surface and improving the material removal rate. These characteristics of ICP help to achieve a uniform etching effect, and by adjusting the ratio of RF power and gas flow, the etching process can be precisely controlled to ensure the controllability and adaptability of the process. In addition, the strong compatibility of ICP technology with existing semiconductor manufacturing processes enables PASE technology to be quickly integrated into existing production lines, providing an ideal plasma source for efficient and high-quality silicon wafer polishing.

PASE uses high-energy particles (mainly ions and free radicals) in plasma to react chemically with the surface of a material, thereby selectively removing the surface material, which is the same as the reaction principle in PCVM. For different substrate materials, different reaction gases are selected according to the chemical reaction that can occur on the substrate's surface. In addition, in PCVM, helium is usually used as the working gas to ensure the generation and stability of plasma; while in PASE, due to the high energy density of ICP, argon can be selected as the working gas, and so there is physical etching occurring at the same time during the processing process. PASE combines physical etching and chemical reactions with high selectivity and precision.

For processing Si substrates, Fang et al. [75] achieved surface polishing by using a self-designed PASE device, as shown in **Figure 11a**. The torch tube of the device adopted a combined structure, which was divided into two layers: the inner layer was mainly used to introduce the reaction gas (mainly CF_4 and O_2) and the auxiliary gas (Ar), and the outer layer was responsible for the introduction of the cooling gas (Ar). When the auxiliary gas entered the torch tube, the ignition device discharged the gas to generate seed electrons. The argon gas carrying the seed electrons then flowed into the induction coil area, and the RF power supply was coupled through the matcher and input into the coil. The seed electrons in the auxiliary gas were accelerated in the induction coil area and interacted with the argon atoms, eventually causing the argon gas to ionize and form plasma. Subsequently, the reaction gas was introduced into the plasma and decomposed to produce fluorine atoms using the principle of chemical reaction. These fluorine atoms reacted with silicon atoms on the surface of the single-crystal silicon, thereby achieving material removal. Specifically, the original surface of the polished single-crystal silicon wafer was usually rough and had many protrusions. There were various silicon atoms with dangling bonds on the surface of these protrusions, and the number of dangling bonds ranged from one to three. Through computational analysis, it was found that silicon atoms with different numbers of dangling bonds had different priorities during the etching process. Silicon atoms with more dangling bonds required lower activation energy to form SiF_4 molecules. Therefore, single-crystal silicon atoms with three dangling bonds had the highest chemical reactivity and preferentially combined with chemically reactive fluorine atoms in the plasma, as shown in **Figure 11b**. As this selective etching process proceeded, the bumps on the rough surface of the single-crystal silicon gradually smoothed out.

For processing GaN substrates, Zhang et al. [76] also used the above-mentioned device, with CF_4 as the reaction gas and Ar as the auxiliary and cooling gas to achieve efficient and damage-free polishing of the substrate's surface, as shown in **Figure 11c**. After the PASE treatment, surface roughness S_a was reduced from 135.8 nm to 0.527 nm, and the MRR reached 93.01 μm/min. PASE also exhibited selective etching when treating GaN. For the GaN substrate, its rough surface was composed of many atomic steps, in which the atoms can be divided into step edge atoms and step surface atoms. Due to the different bond states of these atoms, the chemical activity of these atoms also showed differences, resulting in different removal rates of different atoms. The horizontal etching rate was higher than the vertical etching rate, resulting in the planarization of the GaN substrate's surface, as shown in **Figure 11d**.

For processing SCD substrates, Liu et al. [77] used O_2 as the reaction gas and Ar as the auxiliary and cooling gas, and they selectively etched carbon atoms on the surface of single-crystal diamond (SCD) through active oxygen radicals generated by ICP to finally obtain an atomic-scale smooth surface. The MRR reached up to 56.533 μm/min, and surface roughness S_a was stable at about 0.5 nm. During the polishing process, active oxygen radicals preferentially removed carbon atoms with more dangling bonds on the SCD's surface. Since there were three carbon atoms with dangling bonds, only one C-C bond needed to be broken to form a carbon oxide molecule. Therefore, active oxygen radicals tended to react with carbon atoms with three dangling bonds first. Once a CO/CO_2 molecule was formed, it separated from the wafer's surface and one carbon atom was removed. Due to the different number of dangling bonds of different carbon atoms on the SCD's surface, the removal priority of carbon atoms was different. As the PASE process proceeded, the surface of the SCD underwent several steps to remove carbon atoms with different priorities to eliminate the non-equilibrium state. Finally, all carbon atoms on the SCD's surface had the same bonding state and an atomically balanced and smooth surface form, as shown in **Figure 11e**.

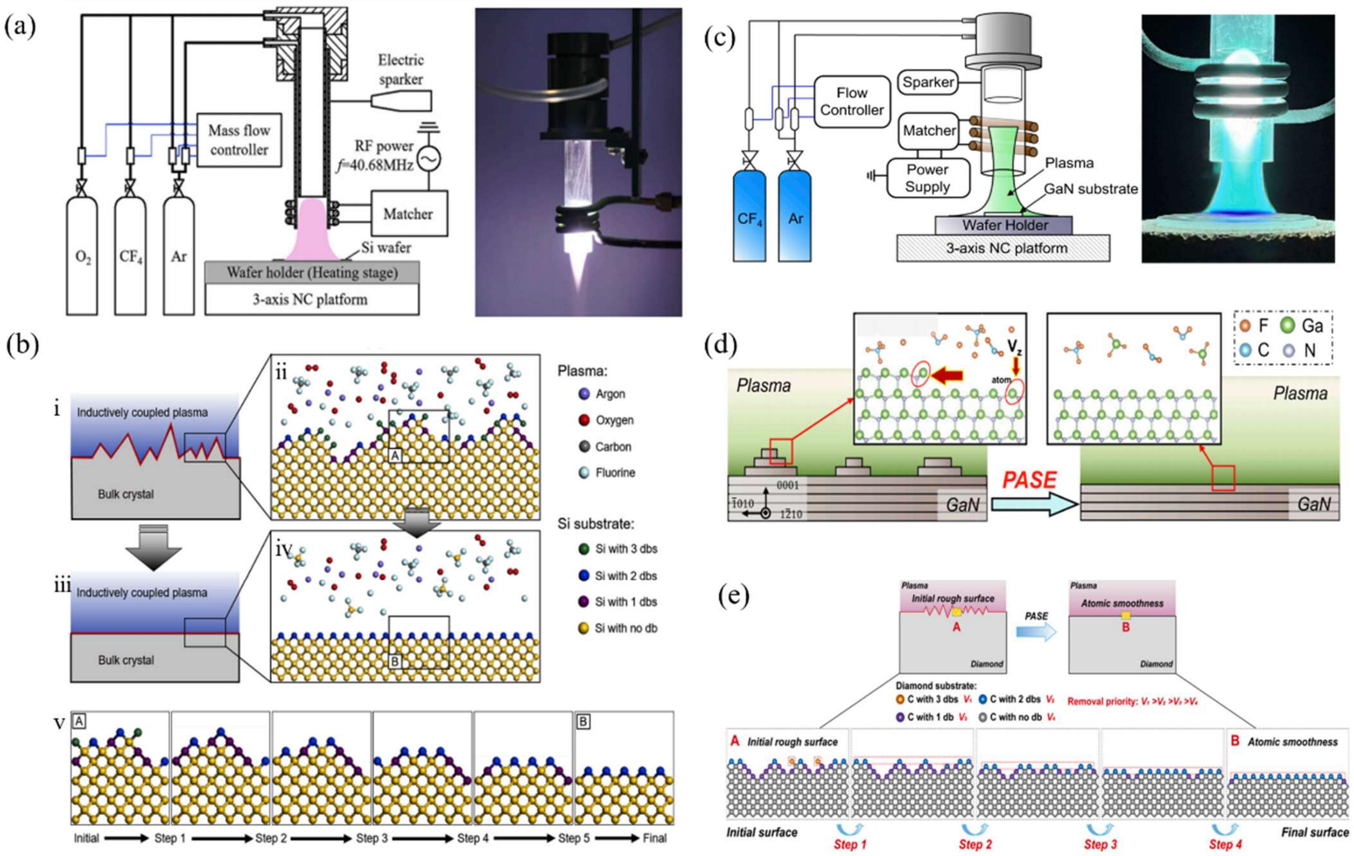

Figure 11. (a) Treatment of Si substrate by PASE device [75]; **(b)** Selective etching process on surface of Si substrate [75]; **(c)** Treatment of GaN substrate by PASE device [76]; **(d)** Selective etching process on surface of GaN substrate [76]; **(e)** Selective etching process on surface of SCD substrate [77].

(2) Impact of different process parameters on PASE technology

PASE also relies on active species in plasma to complete substrate polishing. Therefore, increasing the plasma active species content and energy density is the key to achieving a high MRR. Zhang et al. [76] found that when processing a GaN substrate, the sample's surface temperature and C_2 radical peak intensity increased with the increase in RF power, as shown in **Figure 12a**. A high RF power increased the energy of the plasma, accelerated the dissociation of CF_4 and increased the concentration of F radicals. When the RF power was low, the surface temperature was too low to allow reaction products to volatilize and escape from the surface. The etching products were deposited on the substrate's surface, inhibiting the continuation of the reaction. In addition, an increase in the CF_4 flow rate led to an increase in the peak intensity of C_2 radicals, as shown in **Figure 12b**, indicating that the degree of dissociation of CF_4 molecules increased with the increase in the flow rate, thereby increasing the concentration of F radicals in the plasma. However, if the CF_4 flow rate was too large, it may lead to an excess concentration of radicals in the plasma. The MRR from PASE increased with the increase in surface temperature and the CF_4 flow rate, as shown in **Figure 12c**. Liu et al. [77] found that the concentration of active oxygen radicals in the plasma increased with the increase in the O_2 flow rate when processing SCD, as shown in **Figure 12d**. These highly active oxygen radicals reacted with carbon atoms on the surface of SCD to form CO or CO_2, thereby improving the MRR. However, too high of an O_2 flow rate may cause overheating or over-etching of the SCD's surface, affecting the surface quality.

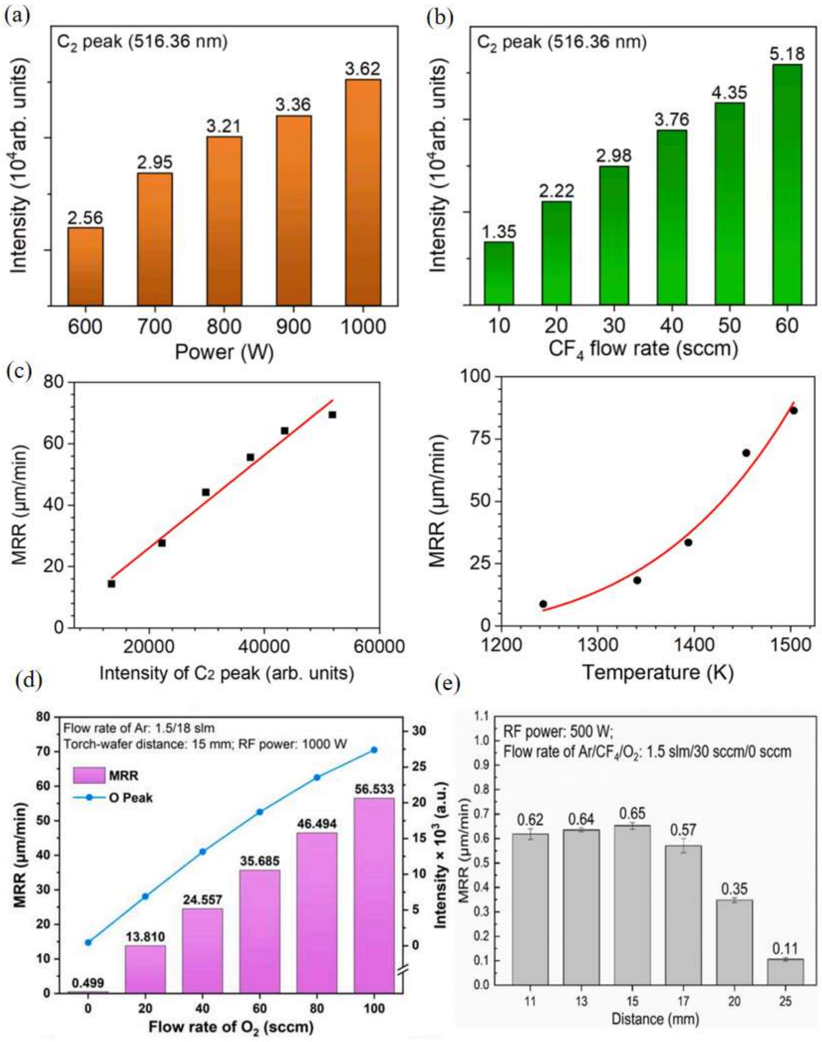

Figure 12. (a) Variation of C_2 radical peak intensity with RF power [76]; **(b)** Variation of C_2 radical peak intensity with CF_4 flux [76]; **(c)** Variation of MRR with C_2 radical peak intensity and substrate temperature [76]; **(d)** Variation of MRR with reactive oxygen radical concentration with O_2 flux [77]; **(e)** Variation of MRR with distance between plasma torch tube and sample [75].

In addition, due to the particularity of the ICP device structure used in PASE, the distance between the plasma torch and the substrate also affects the processing. Fang et al. [74] and Fang [75] adjusted the distance between the plasma torch and the wafer and found that when the distance was less than 15 mm, the MRR showed an upward trend with the increase in the distance. This phenomenon can be attributed to the fact that the operation was carried out in an atmospheric environment, and the oxygen in the air helped to promote the plasma etching process. However, during the polishing process, the flow of argon gas as a cooling gas caused some interference with the oxygen in the atmosphere that participated in the etching reaction. When the torch was close to the wafer's surface, the argon gas formed a certain barrier to oxygen, limiting the role of oxygen in the atmosphere in the plasma, resulting in a decrease in the MRR. When the distance exceeded 15 mm, the MRR began to decrease. Although the oxygen in the air could fully participate in the reaction, the increase in the distance between the plasma and the sample caused the temperature of the etching reaction area to decrease, thereby slowing down the etching reaction rate. In addition, due to the limited lifetime of the active particles in the plasma, the concentration of the active particles participating in the reaction also decreased with the increase in distance, which further led to a decrease in the MRR. Therefore, under the combined effect of multiple factors, the increase in the distance between the plasma torch and the sample caused the material removal rate to show a trend of first increasing and then decreasing, as shown in **Figure 12e**.

(3) Summary

At this stage, PASE technology shows high selectivity, high precision, multi-material adaptability and stability, and it has been widely used in a variety of semiconductor materials, such as silicon, gallium nitride and diamond. By optimizing gas mixing and process parameters, nanometer-level etching accuracy has been achieved. However, with the continuous advancement of chip manufacturing technology, PASE technology faces new challenges and development directions. The development of PASE technology will focus on improving the etching rate and uniformity, continuing to optimize the plasma source and process parameters, further shortening the processing time, improving production efficiency and ensuring consistent etching quality for large-area wafers. With the development of heterogeneous integration technology, PASE needs to adapt to the etching of more types and more complex structures of materials to ensure high selectivity and high-precision etching of different materials and structural layers. In terms of environmental protection, PASE technology will develop in the direction of green environmental protection via studies on the use of more environmentally friendly process gases, the reduction of the use and emission of harmful gases and the reduction of the impact on the environment. In addition, by optimizing the plasma source and process parameters, energy consumption can be reduced to achieve a greener and more energy-saving etching process. In addition, intelligence and automation will become important development trends of PASE technology in the future. Introducing artificial intelligence and machine learning technology can help realize the intelligent control of the plasma etching process and further improve etching accuracy and process stability. Furthermore, highly automated plasma etching production lines can be developed to achieve full automation from the process parameter setting to the etching process for improving production efficiency and quality consistency.

2.3. Comparison of plasma chip-polishing technologies

In modern manufacturing, plasma polishing technology has attracted widespread attention due to its superior surface treatment capabilities. The choice of polishing technology directly affects the surface quality and final performance of products. In **Table 4**, the above-mentioned four main plasma polishing technologies are compared and summarized.

Table 4. Comparison of plasma-related chip-polishing technologies.

Type of process	**Material removal rate (MRR, μm/h)**	**Surface roughness (S_q, nm)**	**References**
Plasma-assisted polishing (PAP)	0.06–2.1	0.08–2.40	[25,54–62]
Plasma electrolytic processing-mechanical polishing (PEP-MP)	2.3–21.8	0.23–0.81	[64]
Plasma chemical vaporization machining (PCVM)	100–550	0.80–0.92	[69,71]
Plasma assisted selective etching (PASE)	3391.98–5580.60	0.60–0.74	[75,76]

PAP and PEP-MP are indirect processing technologies, which use plasma treatment first and then mechanical polishing, and both can treat a large area of a substrate at the same time. PAP is a technology that alternates direct plasma modification of a substrate’s surface and mechanical polishing. The advantage of PAP technology lies in its precise surface treatment and less damage to the base material. However, PAP has certain difficulties in uniformly processing complex shapes. PEP-MP adopts the process of plasma electrolytic treatment first to generate a softening layer, followed by mechanical polishing. The significant advantages of PEP-MP are its high removal rate and ability to handle complex-shaped surfaces. However, the continuous growth of the softening layer may lead to poor surface quality. In addition, the current application of PEP-MP mainly focuses on SiC materials, and hence its application scope needs to be broadened.

As direct plasma processing technologies, PCVM and PASE have MRRs that are several orders of magnitude higher than those of indirect processing technologies. However, their processing area is limited, which results in a longer processing time for large-area substrates. PCVM technology has a wide range of applications, but the equipment is complex and has high safety requirements for gas treatment. PASE uses the etching effect of ICP plasma to complete the treatment of a substrate. Its advantage lies in selective etching and is suitable for surface treatment of a variety of materials. However, accurately controlling the energy density of plasma and the reaction process on a substrate’s surface to surpass the surface roughness accuracy achieved by indirect processing technology is still a key issue that PVCM and PASE need to solve.

3. Summary and outlook

With the rapid development of semiconductor technology, chip polishing technology is also undergoing constant innovation and optimization. As traditional processes, MP and CMP have gradually shown their limitations in removing micro-scale defects and impurities. In response to these problems, researchers have developed a variety of plasma polishing technologies, such as PAP, PEP-MP, PCVM and PASE, in order to achieve more efficient and finer surface treatment effects. Although traditional polishing technologies can remove the raised parts of a surface and make the surface reach the required flatness and smoothness, these methods gradually reveal their limitations when facing the removal of micro-scale defects and impurities, such as mechanical grinding causing surface scratches and subsurface damage, thereby affecting the integrity and service life of a material's surface, as well as a low material removal rate, which requires longer processing time and leads to reduced production efficiency.

Low-temperature plasma technology with efficient processing and green environmental protection has brought a new breakthrough in chip surface treatment. The highly ionized characteristics of low-temperature plasma enable it to interact with a chip's surface, accurately remove tiny defects and roughness on the chip's surface and improve the flatness and finish of the chip. Compared with traditional chip polishing technologies, low-temperature plasma technology can reduce mechanical damage to a chip's surface, will not introduce sub-surface damage and has a higher material removal rate. It can complete the chip polishing process in a shorter time and improve production efficiency.

Based on the traditional chip polishing process, the PAP process uses plasma to replace other technologies for generating a softening layer, and then it uses mechanical polishing to remove it, thereby achieving a flat surface. PAP reduces the use of a large number of chemical reagents and is used in the field of surface polishing of various chip materials. In the future, the development of high-activity plasma sources, as well as research on coupling with mechanical polishing processes, should be strengthened to improve the stability and efficiency of PAP to achieve efficient and accurate surface treatment. In the PEP-MP process, PEP is widely used in the field of surface polishing of metal parts, but it is less studied in the field of surface polishing of chip materials. In the future, it is necessary to broaden its application scope and deepen the research on the growth mechanism of its softening interface layer in order to achieve more precise regulation. PCVM eliminates the process of mechanical polishing and is used for efficient and fast processing of a chip material's surface. Due to the limited processing area of a plasma source, PCVM takes longer to process large-area substrates. Therefore, it is necessary to develop a large-area, high-stability, and high-uniformity plasma source to achieve large-scale applications. The PASE process is based on the principle of selective etching and can achieve highly selective and precise surface rapid processing. In the future, by introducing various technologies, such as intelligent control, more precise control of plasma process parameters can be achieved to achieve uniform processing of large-size substrates.

If low-temperature plasma technology can be combined with other disciplines, such as nanomaterials science and surface engineering, new polishing mechanisms and methods may be generated and significant progress may be made: with the support of nanomaterials science, plasma polishing processes may develop more precise material removal mechanisms, achieve a high degree of control over microstructures and achieve nanoscale surface processing with higher precision and low damage; with the support of surface engineering technology, the surface of a polished chip material may have functional characteristics, such as low roughness and high bonding strength, in addition to improving the overall performance and expanding the scope of application. Furthermore, the interdisciplinary combination will help promote the industrial application of low-temperature plasma technology in the chip industry, develop low-cost and high-efficiency equipment and provide new technical support for high-end manufacturing.

The application of low-temperature plasma in chip polishing is expected to push the manufacturing of microelectronic devices further toward the nanoscale, achieving higher integration and lower power consumption. Also, with the development of emerging technologies, such as quantum computing and artificial intelligence, the requirements for chip performance and manufacturing processes will become more stringent, which will make the role of low-temperature plasma technology in chip manufacturing more critical, and this is expected to help the global electronics industry achieve a higher level of competitiveness and innovation.

Author contributions: Conceptualization, RW and LQ; methodology, RW, LQ, HY, SX and PG; investigation, HY, SX, PG, JH, GW and YZ; writing—original draft preparation, HY, SX, PG, JH, GW and YZ; writing—review and editing, HY, SX and PG; visualization, HY, SX and PG; supervision, RW and LQ; project administration, RW and LQ; funding acquisition, RW. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Beijing Natural Science Foundation (JQ23013), Fundamental Research Funds for the Central Universities (buctrc201906) and Beijing Nova Program (2022015,20230484449).

Conflict of interest: The authors declare no conflict of interest.

References

1. Zhang H, Qu Z, Tang H, et al. On-Chip Integration of a Covalent Organic Framework-Based Catalyst into a Miniaturized Zn–Air Battery with High Energy Density. ACS Energy Letters. 2021; 6(7): 2491-2498. doi: 10.1021/acsenergylett.1c00768
2. Qi D, Liu Y, Liu Z, et al. Design of Architectures and Materials in In-Plane Micro-supercapacitors: Current Status and Future Challenges. Advanced Materials. 2016; 29(5). doi: 10.1002/adma.201602802
3. Peng Y, Akuzum B, Kurra N, et al. All-MXene (2D titanium carbide) solid-state microsupercapacitors for on-chip energy storage. Energy & Environmental Science. 2016; 9(9): 2847-2854. doi: 10.1039/c6ee01717g
4. Song Y, Wang J, Liang L. Thickness effect on the mechanical performance of cathodes in lithium-ion batteries. Journal of Energy Storage. 2024; 86: 111417. doi: 10.1016/j.est.2024.111417
5. Chaniotakis N, Sofikiti N. Novel semiconductor materials for the development of chemical sensors and biosensors: A review. Analytica Chimica Acta. 2008; 615(1): 1-9. doi: 10.1016/j.aca.2008.03.046
6. Li Q. Integrated Circuit Chip Manufacturing Technology and Process Analysis (Chinese). Digital Technology & Application. 2023; 41(12): 46-48. doi: 10.19695/j.cnki.cn12-1369.2023.12.14
7. Lyons JL, Wickramaratne D, Janotti A. Dopants and defects in ultra-wide bandgap semiconductors. Current Opinion in Solid State and Materials Science. 2024; 30: 101148. doi: 10.1016/j.cossms.2024.101148
8. Jiang K, Zhang P, Song S, et al. A review of ultra-short pulse laser micromachining of wide bandgap semiconductor materials: SiC and GaN. Materials Science in Semiconductor Processing. 2024; 180: 108559. doi: 10.1016/j.mssp.2024.108559

9. Zhang Q. Research on the development of China’s third-generation semiconductor industry (Chinese). Science and Technology Square. 2024; 2: 19-25. doi: 10.13838/j.cnki.kjgc.2024.02.008
10. Casady JB, Johnson RW. Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review. Solid-State Electronics. 1996; 39(10): 1409-1422. doi: 10.1016/0038-1101(96)00045-7
11. Hu D, Lin Q, Wu H, et al. Exploration of semiconductor technology development trends—Taking RF power amplifiers as an example (Chinese). Journal of Guilin University of Electronic Technology. 2023; 43(4): 271-281. doi：10.16725/j.cnki.cn45-1351/tn.2023.04.001
12. Zhang Y, Zhang Q. SiC chip miniaturization and development trend (Chinese). Electric Drive for Locomotives. 2023; 5: 46-62. doi: 10.13890/j.issn.1000-128X.2023.05.005
13. Srivastava M, Singh J, Mishra DK, et al. Review on the various strategies adopted for the polishing of silicon wafer—A chemical perspective. Materials Today: Proceedings. 2022; 63: 62-68. doi: 10.1016/j.matpr.2022.02.300
14. Dong Z, Lin Y. Ultra-thin wafer technology and applications: A review. Materials Science in Semiconductor Processing. 2020; 105: 104681. doi: 10.1016/j.mssp.2019.104681
15. Zhang R, Yu X, Cheng R, et al. Progress and Trends in Integrated Circuit Advanced Manufacturing Technology (Chinese). Frontiers of Data & Computing. 2021; 3(5): 28-39.
16. Dranczewski J, Fischer A, Tiwari P, et al. Plasma etching for fabrication of complex nanophotonic lasers from bonded InP semiconductor layers. Micro and Nano Engineering. 2023; 19: 100196. doi: 10.1016/j.mne.2023.100196
17. Baek KH, Edgar TF, Song K, et al. An effective procedure for sensor variable selection and utilization in plasma etching for semiconductor manufacturing. Computers & Chemical Engineering. 2014; 61: 20-29. doi: 10.1016/j.compchemeng.2013.09.016
18. Qin Y, Zhao C, Gao F. Multi-stage Process Analysis and Modelling based Online Monitoring for Chip Packaging Process. IFAC-PapersOnLine. 2015; 48(28): 993-998. doi: 10.1016/j.ifacol.2015.12.260
19. Kong X, Li S, Li H, et al. Distribution patterns of reactive species in the interaction between atmospheric pressure plasma jet and fiber membrane. Plasma Sources Science and Technology. 2023; 32(10): 105004. doi: 10.1088/1361-6595/acfd5b
20. Kong X, Li H, Yang W, et al. Atmospheric pressure plasma jet impinging on fiber arrays: Penetration pattern determined by fiber spacing. Applied Physics Letters. 2023; 122(8). doi: 10.1063/5.0139361
21. Ma G, Li S, Liu F, et al. A Review on Precision Polishing Technology of Single-Crystal SiC. Crystals. 2022; 12(1): 101. doi: 10.3390/cryst12010101
22. Li Z, Jiang F, Jiang Z, et al. Energy beam-based direct and assisted polishing techniques for diamond: A review. International Journal of Extreme Manufacturing. 2023; 6(1): 012004. doi: 10.1088/2631-7990/acfd67
23. Geng Z, Huang N, Castelli M, et al. Polishing Approaches at Atomic and Close-to-Atomic Scale. Micromachines. 2023; 14(2): 343. doi: 10.3390/mi14020343
24. Zong WJ, Cheng X, Zhang JJ. Atomistic origins of material removal rate anisotropy in mechanical polishing of diamond crystal. Carbon. 2016; 99: 186-194. doi: 10.1016/j.carbon.2015.12.001
25. Luo Q, Lu J, Xu X, et al. Removal mechanism of sapphire substrates (0001, $11\bar{2}0$ and $10\bar{1}0$) in mechanical planarization machining. Ceramics International. 2017; 43(18): 16178-16184. doi: 10.1016/j.ceramint.2017.08.194
26. Kubota A, Fukuyama S, Ichimori Y, et al. Surface smoothing of single-crystal diamond (100) substrate by polishing technique. Diamond and Related Materials. 2012; 24: 59-62. doi: 10.1016/j.diamond.2011.10.022
27. Kubota A, Nagae S, Touge M. Improvement of material removal rate of single-crystal diamond by polishing using H_2O_2 solution. Diamond and Related Materials. 2016; 70: 39-45. doi: 10.1016/j.diamond.2016.09.028
28. Tatsumi N, Harano K, Ito T, et al. Polishing mechanism and surface damage analysis of type IIa single crystal diamond processed by mechanical and chemical polishing methods. Diamond and Related Materials. 2016; 63: 80-85. doi: 10.1016/j.diamond.2015.11.021
29. Li Q, Liu L, Yu J, et al. Investigation on chemical mechanical polishing of Ga-faced GaN crystal with weak alkaline slurry. Applied Surface Science. 2024; 653: 159396. doi: 10.1016/j.apsusc.2024.159396
30. Deng H, Hosoya K, Imanishi Y, et al. Electro-chemical mechanical polishing of single-crystal SiC using CeO_2 slurry. Electrochemistry Communications. 2015; 52: 5-8. doi: 10.1016/j.elecom.2015.01.002

31. Hu Y, Shi D, Hu Y, et al. Investigation on the Material Removal and Surface Generation of a Single Crystal SiC Wafer by Ultrasonic Chemical Mechanical Polishing Combined with Ultrasonic Lapping. Materials. 2018; 11(10): 2022. doi: 10.3390/ma11102022
32. Chen G, Pan L, Luo H, et al. Chemical mechanical polishing of silicon carbide (SiC) based on coupling effect of ultrasonic vibration and catalysis. Journal of Environmental Chemical Engineering. 2023; 11(5): 111080. doi: 10.1016/j.jece.2023.111080
33. Deng H, Hosoya K, Imanishi Y, et al. Electro-chemical mechanical polishing of single-crystal SiC using CeO_2 slurry. Electrochemistry Communications. 2015; 52: 5-8. doi: 10.1016/j.elecom.2015.01.002
34. Wang L. Research on Electrochemical Mechanical Polishing Process of Silicon Carbide Crystals (Chinese) [Master’s thesis]. Dalian University of Technology; 2022.
35. Sidpara A, Jain VK. Nano–level finishing of single crystal silicon blank using magnetorheological finishing process. Tribology International. 2012; 47: 159-166. doi: 10.1016/j.triboint.2011.10.008
36. Ma X, Tian Y, Qian C, et al. Experimental investigation on magnetorheological shear thickening polishing characteristics for SiC substrate. Ceramics International. 2024; 50(20): 40069-40078. doi: 10.1016/j.ceramint.2024.07.392
37. Jang KI, Nam E, Lee CY, et al. Mechanism of synergetic material removal by electrochemomechanical magnetorheological polishing. International Journal of Machine Tools and Manufacture. 2013; 70: 88-92. doi: 10.1016/j.ijmachtools.2013.03.011
38. Saraswathamma K, Jha S, Venkateswara Rao P. Rheological behaviour of Magnetorheological polishing fluid for Si polishing. Materials Today: Proceedings. 2017; 4(2): 1478-1491. doi: 10.1016/j.matpr.2017.01.170
39. Yin T, Zhao P, Doi T, et al. Effect of Using High-Pressure Gas Atmosphere with UV Photocatalysis on the CMP Characteristics of a 4H-SiC Substrate. ECS Journal of Solid State Science and Technology. 2021; 10(2): 024010. doi: 10.1149/2162-8777/abe7a8
40. Lu J, Wang Y, Luo Q, et al. Photocatalysis assisting the mechanical polishing of a single-crystal SiC wafer utilizing an anatase TiO_2-coated diamond abrasive. Precision Engineering. 2017; 49: 235-242. doi: 10.1016/j.precisioneng.2017.02.011
41. Kawabata Y, Taniguchi J, Miyamoto I. XPS studies on damage evaluation of single-crystal diamond chips processed with ion beam etching and reactive ion beam assisted chemical etching. Diamond and Related Materials. 2004; 13(1): 93-98. doi: 10.1016/j.diamond.2003.09.005
42. Luo Q, Chen J, Cheng Z, Lu J. Research progress and development trend of grinding and polishing technology of silicon carbide substrate (Chinese). Journal of Hunan University (Natural Sciences). 2024; 51(4): 140-152. doi： 10.16339/j.cnki.hdxbzkb.2024180
43. Niu S, Chen Y, Wang Y, et al. Chemical mechanical polishing process of gallium nitride chips (Chinese). Science Technology and Engineering. 2020; 20(19): 7639-7643.
44. Sun X, Li J, Zhang W, et al. Research progress on material removal non-uniformity in chemical mechanical polishing of silicon carbide (Chinese). Journal of Synthetic Crystals. 2024; 53(4): 585-599. doi: 10.16553/j.cnki.issn1000-985x.20240013.001
45. Xu H, Wang J, Li Q, Pan F. Research progress in chemical mechanical polishing of silicon carbide wafers (Chinese). Modern Manufacturing Engineering. 2022; 6: 153-161+116.
46. Li Y. Experimental Study on Optimization of Chemical Mechanical Polishing Process for Silicon Carbide Wafer (Chinese) [Master’s thesis]. Henan University of Technology; 2023.
47. Li H, Ren K, Yin Z, et al. A review of research on ultrasonic vibration assisted abrasive flow polishing technology (Chinese). Journal of Mechanical Engineering. 2021; 57(9): 233-253.
48. Chen G, Xiao Q. Research progress on polishing process of single crystal sapphire substrate (Chinese). Tool Engineering. 2018; 52(3): 3-9. doi: 10.16567/j.cnki.1000-7008.2018.03.001
49. Tang A. Research on the Mechanism of Vibration Assisted Photocatalytic Polishing of Silicon Carbide (Chinese) [Master’s thesis]. Shenyang University of Technology; 2023.
50. Zhu X, Gui Y, Fu H, et al. Photocatalytic assisted chemical mechanical polishing for silicon carbide using developed ceria coated diamond core-shell abrasives. Tribology International. 2024; 197: 109827. doi: 10.1016/j.triboint.2024.109827
51. Xiao H, Dai Y, Duan J, et al. Material removal and surface evolution of single crystal silicon during ion beam polishing. Applied Surface Science. 2021; 544: 148954. doi: 10.1016/j.apsusc.2021.148954
52. Mi S, Toros A, Graziosi T, et al. Non-contact polishing of single crystal diamond by ion beam etching. Diamond and Related Materials. 2019; 92: 248-252. doi: 10.1016/j.diamond.2019.01.007

53. Yamamura K, Takiguchi T, Ueda M, et al. High-Integrity Finishing of 4H-SiC (0001) by Plasma-Assisted Polishing. Advanced Materials Research. 2010; 126-128: 423-428. doi: 10.4028/www.scientific.net/amr.126-128.423
54. Deng H, Yamamura K. Atomic-scale flattening mechanism of 4H-SiC (0001) in plasma assisted polishing. CIRP Annals. 2013; 62(1): 575-578. doi: 10.1016/j.cirp.2013.03.028
55. Deng H, Ueda M, Yamamura K. Characterization of 4H-SiC (0001) surface processed by plasma-assisted polishing. The International Journal of Advanced Manufacturing Technology. 2014; 72: 1-7. doi: 10.1007/s00170-012-4430-7
56. Ji J, Yamamura K, Deng H. Plasma assisted polishing technology for manufacturing single-crystal SiC atomic level surfaces (Chinese). Acta Physica Sinica. 2021; 70(6): 74-86.
57. Sun R, Yang X, Arima K, et al. High-quality plasma-assisted polishing of aluminum nitride ceramic. CIRP Annals. 2020; 69(1): 301-304. doi: 10.1016/j.cirp.2020.04.096
58. Deng H, Endo K, Yamamura K. Plasma-assisted polishing of gallium nitride to obtain a pit-free and atomically flat surface. CIRP Annals. 2015; 64(1): 531-534. doi: 10.1016/j.cirp.2015.04.002
59. Peguiron A, Moras G, Walter M, et al. Activation and mechanochemical breaking of C–C bonds initiate wear of diamond (110) surfaces in contact with silica. Carbon. 2016; 98: 474-483. doi: 10.1016/j.carbon.2015.10.098
60. Yamamura K, Emori K, Sun R, et al. Damage-free highly efficient polishing of single-crystal diamond wafer by plasma-assisted polishing. CIRP Annals. 2018; 67(1): 353-356. doi: 10.1016/j.cirp.2018.04.074
61. Luo H, Ajmal KM, Liu W, et al. Atomic-scale and damage-free polishing of single crystal diamond enhanced by atmospheric pressure inductively coupled plasma. Carbon. 2021; 182: 175-184. doi: 10.1016/j.carbon.2021.05.062
62. Liu N, Sugimoto K, Yoshitaka N, et al. Effects of polishing pressure and sliding speed on the material removal mechanism of single crystal diamond in plasma-assisted polishing. Diamond and Related Materials. 2022; 124: 108899. doi: 10.1016/j.diamond.2022.108899
63. Nestler K, Böttger-Hiller F, Adamitzki W, et al. Plasma Electrolytic Polishing – An Overview of Applied Technologies and Current Challenges to Extend the Polishable Material Range. Procedia CIRP. 2016; 42: 503-507. doi: 10.1016/j.procir.2016.02.240
64. Huang Y, Wang C, Ding F, et al. Principle, process, and application of metal plasma electrolytic polishing: a review. The International Journal of Advanced Manufacturing Technology. 2021; 114(7-8): 1893-1912. doi: 10.1007/s00170-021-07012-7
65. Ma G, Li S, Liu X, et al. Combination of Plasma Electrolytic Processing and Mechanical Polishing for Single-Crystal 4H-SiC. Micromachines. 2021; 12(6): 606. doi: 10.3390/mi12060606
66. Zhang C. Simulation and Experimental Study on Ultrasonic Assisted Electrolyte Plasma Polishing of SiC Single Crystal (Chinese) [Master's thesis]. Xi'an University of Technology; 2023. pp. 13-20.
67. Liu N, Yi R, Deng H. Study of initiation and development of local oxidation phenomena during anodizing of SiC. Electrochemistry Communications. 2018; 89: 27-31. doi: 10.1016/j.elecom.2018.02.013
68. Chen Y, Yi J, Wang Z, et al. Experimental study on ultrasonic-assisted electrolyte plasma polishing of SUS304 stainless steel. The International Journal of Advanced Manufacturing Technology. 2022; 124(7-8): 2835-2846. doi: 10.1007/s00170-022-10646-w
69. Sano Y, Watanabe M, Yamamura K, et al. Polishing Characteristics of Silicon Carbide by Plasma Chemical Vaporization Machining. Japanese Journal of Applied Physics. 2006; 45(10B): 8277. doi: 10.1143/jjap.45.8277
70. Nakahama Y, Kanetsuki N, Funaki T, et al. Etching characteristics of GaN by plasma chemical vaporization machining. Surface and Interface Analysis. 2008; 40(12): 1566-1570. doi: 10.1002/sia.2955
71. Yamamura K, Yamamoto Y, Deng H. Preliminary Study on Chemical Figuring and Finishing of Sintered SiC Substrate Using Atmospheric Pressure Plasma. Procedia CIRP. 2012; 3: 335-339. doi: 10.1016/j.procir.2012.07.058
72. Nakanishi Y, Mukai R, Matsuyama S, et al. Cause of Etch Pits during the High Speed Plasma Etching of Silicon Carbide and an Approach to Reduce their Size. Materials Science Forum. 2020; 1004: 161-166. doi: 10.4028/www.scientific.net/msf.1004.161
73. Ueda M, Shibahara M, Zettsu N, et al. Effect of Substrate Heating in Thickness Correction of Quartz Crystal Wafer by Plasma Chemical Vaporization Machining. Key Engineering Materials. 2010; 447-448: 218-222. doi: 10.4028/www.scientific.net/kem.447-448.218

74. Fang Z, Zhang Y, Li R, et al. An efficient approach for atomic-scale polishing of single-crystal silicon via plasma-based atom-selective etching. International Journal of Machine Tools and Manufacture. 2020; 159: 103649. doi: 10.1016/j.ijmachtools.2020.103649
75. Fang Z. Study on the Process of Atmospheric Pressure Plasma Lateral Etching and Polishing of Single Crystal Silicon Wafers (Chinese) [Master's thesis]. Harbin Institute of Technology; 2020.
76. Zhang L, Wu B, Zhang Y, et al. Highly efficient and atomic scale polishing of GaN via plasma-based atom-selective etching. Applied Surface Science. 2023; 620: 156786. doi: 10.1016/j.apsusc.2023.156786
77. Liu W, Xiao Y, Zhang Y, et al. Highly efficient and atomic-scale smoothing of single crystal diamond through plasma-based atom-selective etching. Diamond and Related Materials. 2024; 143: 110840. doi: 10.1016/j.diamond.2024.110840